

# Implementation of Grayscale Image Segmentation Based on FPGA

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## ABSTRACT

An automatic multilevel thresholding algorithm called HVEM (Histogram-based Valley Estimation Method) based on field programmable gate array (FPGA) is presented for segmenting an image into multiple regions with a similar gray-level distribution. The proposed method is computationally efficient so that it can be easily implemented on an FPGA circuit. A method for determining cluster number is also introduced to automatically choose the proper number of thresholds by estimating all possible valleys in a histogram. The proposed method was compared with the Otsu method on a large number of images. In contrast to HVEM, Otsu's method has a serious drawback when extending to a multi-threshold version that is very time consuming and also difficult to be implemented on FPGA. Timing simulations show that the designed hardware can run at a speed of 191 MHz (or 1,457 frames per second) for a 256x256 gray-level image. This result confirms that the proposed FPGA architecture can achieve the requirements for a real-time image processing system.

Keywords : Otsu ; HVEM ; FPGA ; Multi-Threshold ; Segmentation

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