一個解決標準晶元模組擺置合理化問題之動態規劃演算法 = A dynamic programming algorithm for legalization in standard cell..

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摘 要

隨著半導體製造技術的日益精進，VLSI電路元件越來越龐大，因此對積體電路前端及後端設計而言，其設計流程亦日趨複雜。以具有標準晶元設計為考量之後端實體設計(physical design)而言，擺置(placement)是一個相當重要的設計階段。其可細分為三大階段，分別為全域擺置(global Placement)、合理化(legalization)和細部擺置(detailed placement)，擺置結果嚴重影響整個後端設計之良窳。 全域擺置是以減少網列(netlist)連線長度及擁擠度等為目標，產生初始電路擺置圖，合理化階段為解決晶元合理擺置問題，以符合電路設計原則，而細部擺置的目的在於微調合理化的電路，使電路效能更加提升。在本論文中，我們提出一個演算法來解決擺置合理化問題，演算法中包含晶元列切割、晶元指派到晶元列內以及利用動態規劃解決各晶元列內晶元位置合理化三大步驟。合理化問題目標為讓晶元總位移量越少越好。 實驗結果顯示所提演算法確實能解決合理化問題，且平均而言在執行時間與結果品質兩方面皆能有不錯之成效。

關鍵詞 : 擺置 ; 實體設計

目錄

參考文獻

[1]Tony F. Chan, Jason Cong, Tianming Kong and Joseph R. Shinnerl(2000) "Multilevel optimization for large-scale circuit placement" IEEE/ACM International Conference on Computer Aided Design, pages 171 - 176.

[2]Jens Vygen (1997) "Algorithms for large-scale flat placement" Design Automation Conference, pages 746 - 751 [3]Ulrich Brenner, Anna Pauli and Jens Vygen (2004) "Almost optimum placement legalization by minimum cost flow and dynamic programming" International Symposium on Physical Design, pages 2 - 9.

[4]Ulrich Brenner and Jens Vygen (2004) "Legalizing a placement with minimum total movement" IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, pages 1597 - 1613.

[5]Sung-Woo Hur and John Lillis (2000) "Mongrel: hybrid techniques for standard cell placement" IEEE/ACM International Conference on Computer Aided Design, pages 165 - 170.

[6]Giancarlo Beraudo and John Lillis (2003) "Timing optimization of FPGA placements by logic replication" Design Automation Conference, pages 196 - 201.

[7]Ameya Agnihotri, Mehmet Can YlLDlZ, Ateen Khatkhate, Ajita Mathur, Satoshi Ono, and Patrick H. Madden (2003) "Fractional cut:

improved recursive bisection placement" IEEE/ACM International Conference on Computer Aided Design, pages 307 - 310.
[8]Andrew B. Kahng, Igor L. Markov and Sherief Reda (2004) "On legalization of row-based placements" ACM Great Lakes Symposium on VLSI, pages 214 - 219.
[9]Tao Luo, Haoxing Ren, Charles J. Alpert, and David Z. Pan (2005) "Computational geometry based placement migration" IEEE/ACM International Conference on Computer Aided Design, pages 41 - 47.
[10]Majid Sarrafzadeh and Maogang Wang (1997) "NRG: global and detailed placement" IEEE/ACM International Conference on Computer Aided Design,1997, pages 532 - 537.
[11]Dwight Hill (2002) "Method and system for high speed detailed placement of cells within an integrated circuit design" United States Patent 6370673.
[12]Haoxing Ren, avid Z. Pan, Charles J. Alpert and Paul Villarrubia (2005) "Diffusion-based placement migration" Design Automation Conference, pages 515 - 520.
[13]林彥劭，標準元件合法化擺置之最小位移研究，碩士論文，逢甲大學資訊工程系，2009。
[14]卓政達，一個解決標準晶元模組擺置合理化問題之建構式演算法，碩士論文，大葉大學電機工程學系，2009。
[15]Ateen Khatkhate, Chen Li, Ameya R. Agnihotri, Mehmet C. Yildiz, Satoshi Ono, Cheng-Kok Koh and Patrick H. Madden (2004) "Recursive bisection based mixed block placement" International Symposium on Physical Design, pages 84 - 89.
[16]Andrew B. Kahng and Qinke Wang (2004) "Implementation and extensibility of an analytic placer" International Symposium on Physical Design, pages 18 - 25.
[17]Andrew B. Kahng, Igor L. Markov and Sherief Reda (2004) "On legalization of row-based placements" ACM Great Lakes Symposium on VLSI, pages 214 - 219.
[18]Bo Yao, Hongyu Chen, Chung-Kuan Cheng, Nan-Chi Chou, Lung-Tien Liu and Peter Suaris (2005) "Unified quadratic programming approach for mixed mode placement" International Symposium on Physical Design, pages 193 - 199.
[19]Jarrod A. Roy and Igor L. Markov (2007) "ECO-System: Embracing the Change in Placement" Asia and South Pacific Design Automation Conference, pages 147 - 152.
[20] http://cad_contest.ee.ntu.edu.tw/cad08/