A Study of Hierarchical Layout Density Control for Chemical－Mechanical Planarization

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ABSTRACT

The Chemical-Mechanical Polishing (CMP) technology is an important procedure in the fabrication of chip to enhance the overall smoothness need for increasing the yield. Insertion of dummy fill is an important issue for CMP planarization in the back-end synthesis flow of IC design. Layout density analysis is the basics to calculate the amount of dummy fill for CMP planarization. In this article, we proposed a hieratical approach of layout density analysis. The proposed hieratical method has the advantages both on efficiency and accuracy for layout density analysis. The experimental results with the ISCAS89 benchmark show that the proposed hieratical method outperforms the Fixed-Dissection Density Analyses approach.

Keywords : layout density analysis、planarization、Chemical-Mechanical Polishing

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REFERENCES

[1]林宗輝、馬光華，「方興未艾之可製造性導向設計」，台灣半導體產業協會簡訊專文，2005/7。

[2]Franklin M. Schellenberg, and Luigi Capodieci,“ Impact of RET on physical layouts, ” in Proc. of the 2001 international symposium on Physical design, 2001,pp. 52 – 55.

[3]Jeong-Taek Kong, “ CAD for Nanometer Silicon Design Challenges and Success, ” IEEE Trans. on VLSI Systems, vol. 12, no. 11, pp. 1132 – 1147, Nov. 2004.
[4]A. B. Kahng and K. Samadi, “ CMP Fill Synthesis: A Survey of Recent Studies, ” IEEE Trans. on CAD, vol. 27, no. 1, pp.3 – 19, Jan. 2008.
[5]R. Tian, D. F. Wong, and R. Boone, “ Model-Based Dummy Feature Placement for Oxide Chemical-Mechanical Polishing Manufacturability, ” in Proc. ACM/IEEE Des. Autom. Conf., 2000, pp. 667 – 670.
[6]Y. Chen, A. B. Kahng, G. Robins and A. Zelikovsky, “ Hierarchical Dummy Fill for Process Uniformity, ” Proc.ASP-DAC, 2001, pp. 139 – 144.
[7]Y. Chen, P. Gupta, and A. B. Kahng, “ Performance-impact limited area fill synthesis, ” in Proc. ACM/IEEE Des. Autom. Conf., 2003, pp. 22 – 27.
[8]A. B. Kahng, G. Robins, A. Singh, and A. Zelikovsky, “ Filling algorithms and analyses for layout density control, ” IEEE Trans. Comput.-Aided Design Integrated. Circuits and systems, vol. 18, no. 4, pp. 445 – 462, Apr. 1999.
[9]H. Xiang, K.-Y. Chao, R. Puri and M. D. F.Wong, “ Is Your Layout Density Verification Exact? - A Fast Exact Algorithm For Density Calculation, ” Proc. ACM/IEEE International Symposium on Physical Design, 2007, pp. 19 – 26.
[10]A. Tsuchiya and H. Onodera Modeling of On-Chip Transmission-Lines ---Impact of Orthogonal Wires, Si Substrate and Dummy Fills--- Microwave Workshops and Exhibition 2007, pp. 143 – 148.
[11]Y. Chen, A.B. Kahng, G. Robins and A. Zelikovsky, “ Area Fill Synthesis for Uniform Layout Density ” , IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 21, no. 10, pp. 1132 – 1147, Oct. 2002.
[12]T. E. Gbondo-Tugbawa, “ Chip-Scale Modeling of Pattern Dependencies in Copper Chemical Mechanical Polishing Process, ” Ph.D. dissertation, Massachusetts Institute of Technology, 2002.
[13]Y. Chen, A. B. Kahng, G. Robins, and A. Zelikovsky, “ Monte-Carlo algorithms for layout density control, ” in Proc. IEEE Asia South Pacific Des. Autom. Conf., 2000, pp. 523 – 528.
[14]H. Xiang, L. Deng, R. Puri, K.-Y. Chao, and M. D. F. Wong, “ Dummy fill density analysis with coupling constraints, ” in Proc. ACM/IEEE Int. Symp. Phys. Des., 2007, pp. 3 – 9.
[15]Y. Chen, A. B. Kahng, G. Robins, A. Zelikovsky and Y. Zheng, “ Area Fill Generation with Inherent Data Volume Reduction, ” Proc. Intl Conf on Design Automation and Test in Europe, 2003, pp. 868-873.
[16]Y. Chen, A. B. Kahng, G. Robins, A. Zelikovsky, and Y. Zheng, “ Compressible area fill synthesis, ” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 24, no. 8, pp. 1169 – 1187, Aug. 2005.
[17]L. He, A. B. Kahng, K. Tam and J. Xiong, “ Simultaneous Buffer Insertion and Wire Sizing Considering Systematic CMP Variation and Random Leff Variation, ” in Proc. of the 2005 International Symposium on Physical Design, 2005, pp.78 – 85.
[18] http://ic.engin.brown.edu/classes/EN160S07/lecture27.ppt.
[19] http://www.flandersdc.be/download/nl/6432728/file/present_agfa.zip-umicore_dc_inspir_tours.