

A Constructive Algorithm for Legalization in Standard Cell Placement

卓政達、程仲勝

E-mail: 9806188@mail.dyu.edu.tw

ABSTRACT

Placement is a very important design step in VLSI physical design. In general, placement can be divided into three steps including global placement, legalization and detailed placement. During legalization step, all cell overlaps have to be removed and a legal placement with minimum perturbation will be produced.

In this paper, a constructive algorithm will be proposed to solve the problem of legalization. The proposed algorithm has three steps including row enumeration, cell assignment and position adjustment. The problem objective is to derive a legalization solution with total displacement as few as possible.

The experimental result shows that the proposed constructive algorithm has good performance even on very large testbenches.

Keywords : Placement、Legalization

Table of Contents

封面內頁	
簽名頁	
授權書	iii
中文摘要	iv
英文摘要	v
誌謝	vi
目錄	vii
圖目錄	ix
表目錄	xiii
第一章 緒論	1
1.1 研究背景與動機	1
1.2 研究方法	1
1.3 論文架構	2
第二章 文獻探討	3
2.1 標準晶元模組合理化演算法	3
2.2 混合模式模組合理化演算法	5
2.3 整合全域擺置與擺置合理化的演算法	6
2.4 利用密度調整搭配動態規劃解決合理化問題	7
2.5 利用區間分割搭配網路流問題解決合理化問題	10
2.6 模擬擴散行為進行疊代解決合理化問題	11
第三章 以建構式演算法解決擺置合理化問題	15
3.1 問題描述	16
3.2 建構式擺置合理化演算法	17
3.3 枚舉可用晶元列區間	18
3.4 模組指派到晶元列內	20
3.4.1 模組移動到最近的可用晶元列與以分區觀點調整模組位置	21
3.4.2 以晶元列觀點調整模組位置	25
3.5 晶元列內細部調整模組前後位置	26
第四章 實驗結果	31
第五章 結論與未來展望	43
參考文獻	44
附錄A	A-1

REFERENCES

- [1] Tony F. Chan, Jason Cong, Tianming Kong and Joseph R. Shinnerl (2000) "Multilevel optimization for large-scale circuit placement" IEEE/ACM International Conference on Computer Aided Design, pages 171 - 176.
- [2] Jens Vygen (1997) "Algorithms for large-scale flat placement" Design Automation Conference, pages 746 - 751 [3] Ulrich Brenner, Anna Pauli and Jens Vygen (2004) "Almost optimum placement legalization by minimum cost flow and dynamic programming" International Symposium on Physical Design, pages 2 - 9.
- [4] Ulrich Brenner and Jens Vygen (2004) "Legalizing a placement with minimum total movement" IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, pages 1597 - 1613.
- [5] Sung-Woo Hur and John Lillis (2000) "Mongrel: hybrid techniques for standard cell placement" IEEE/ACM International Conference on Computer Aided Design, pages 165 - 170.
- [6] Giancarlo Beraudo and John Lillis (2003) "Timing optimization of FPGA placements by logic replication" Design Automation Conference, pages 196 - 201.
- [7] Ameya Agnihotri, Mehmet Can YILDIZ, Ateen Khatkhate, Ajita Mathur, Satoshi Ono, and Patrick H. Madden (2003) "Fractional cut: improved recursive bisection placement" IEEE/ACM International Conference on Computer Aided Design, pages 307 - 310.
- [8] Tao Luo, Haoxing Ren, Charles J. Alpert, and David Z. Pan (2005) "Computational geometry based placement migration" IEEE/ACM International Conference on Computer Aided Design, pages 41 - 47.
- [9] Majid Sarrafzadeh and Maogang Wang (1997) "NRG: global and detailed placement" IEEE/ACM International Conference on Computer Aided Design, 1997, pages 532 - 537.
- [10] Dwight Hill (2002) "Method and system for high speed detailed placement of cells within an integrated circuit design" United States Patent 6370673.
- [11] Haoxing Ren, David Z. Pan, Charles J. Alpert and Paul Villarrubia (2005) "Diffusion-based placement migration" Design Automation Conference, pages 515 - 520.
- [12] Saurabh N. Adya and Igor L. Markov (2002) "Consistent placement of macro-blocks using floorplanning and standard-cell placement" International Symposium on Physical Design, pages 12 - 17.
- [13] Jason Cong and Min Xie (2006) "A robust detailed placement for mixed-size IC designs" Asia and South Pacific Design Automation Conference, pages 188 - 194.
- [14] Kristofer Vorwerk, Andrew Kennings, Doris T. Chen and Laleh Behjat (2007) "Floorplan repair using dynamic whitespace management" ACM Great Lakes Symposium on VLSI, pages 552 - 557.
- [15] Sudip Nag and Kamal Chaudhary (1999) "Post-placement residual-overlap removal with minimal movement" Design, Automation, and Test in Europe Conference, pages 581 - 586.
- [16] Ateen Khatkhate, Chen Li, Ameya R. Agnihotri, Mehmet C. Yildiz, Satoshi Ono, Cheng-Kok Koh and Patrick H. Madden (2004) "Recursive bisection based mixed block placement" International Symposium on Physical Design, pages 84 - 89.
- [17] Andrew B. Kahng and Qinke Wang (2004) "Implementation and extensibility of an analytic placer" International Symposium on Physical Design, pages 18 - 25.
- [18] Andrew B. Kahng, Igor L. Markov and Sherief Reda (2004) "On legalization of row-based placements" ACM Great Lakes Symposium on VLSI, pages 214 - 219.
- [19] Bo Yao, Hongyu Chen, Chung-Kuan Cheng, Nan-Chi Chou, Lung-Tien Liu and Peter Suaris (2005) "Unified quadratic programming approach for mixed mode placement" International Symposium on Physical Design, pages 193 - 199.
- [20] Jarrod A. Roy and Igor L. Markov (2007) "ECO-System: Embracing the Change in Placement" Asia and South Pacific Design Automation Conference, pages 147 - 152.
- [21] Chin-Chih Chang, Jason Cong and Xin Yuan (2003) "Multi-level placement for large-scale mixed-size IC designs" Asia and South Pacific Design Automation Conference, pages 325 - 330.
- [22] Taraneh Taghavi, Xiaojian Yang and Bo-Kyung Choi (2005) "Dragon2005: large-scale mixed-size placement tool" International Symposium on Physical Design, pages 245 - 247.
- [23] http://www.public.iastate.edu/~nataraj/ISPD04_Bench.html [24] http://cad_contest.ee.ntu.edu.tw/cad08/