一個解決標準晶元模組擺置合理化問題之建構式演算法

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摘 要

積體電路後端實體設計(physical design)中，擺置(Placement)一直是一個相當重要的設計階段。擺置階段可分三大步驟，分別為全域擺置(Global Placement)、合理化(Legalization)和詳細擺置(Detailed Placement)，其中合理化步驟解決模組重疊及模組合理擺置問題。

在本論文中，我們提出一個建構式的演算法來解決合理化問題，演算法中包含枚舉可用晶元列區間、模組指派到晶元列內以及晶元列內細部調整模組前後位置三個步驟，如此可將各個模組調整至適當位置對齊晶元列且不與其他模組或障礙區重疊。合理化問題目標為讓總位置移動量越少越好。

實驗結果顯示所提建構式的演算法確實能解決合理化問題，且在大型的電路實驗中仍然維持其效能。

關鍵詞 : 合理化、擺置

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