Incremental Floorplanning by Using Corner Stitching Representation

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ABSTRACT

Floorplanning is a very important step of physical design in the backend of IC design. As VLSI/SOC systems become more complex, it is probably necessary to reperform floorplanning process for obtaining a better solution if the initial result is unsatisfied. However, it is extremely time consuming to repeatedly perform floorplanning process. For this reason, the idea of incremental floorplanning is adopted to shorten the time and achieve quick physical design closure.

In this thesis, we must obtain an initial floorplanning result on any floorplanning representation and record the relative positions among modules by Corner Stitching. To preserve the original positions relationship among modules, a floorplanning will not be reperformed. In fact, a series of incremental operations, including insertion and modification will be performed to derive a floorplanning solution in which chip area is not changed and total routing length is optimal.

Experimental results show that the proposed incremental floorplanning algorithm has good performance especially in dealing with instances with small changes.

Keywords : Corner Stitching、floorplanning、incremental floorplanning

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