植基於Corner stitching表示法之增量式平面規劃之研究

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摘 要

積體電路後端實體設計(physical design)中，平面規劃(floorplanning)一直是一個相當重要的設計步驟。然而隨著VLSI/SOC系統的複雜化，有可能在平面規劃結束後，因佈局結果不良，需重新再進行平面規劃以求得一較佳佈局結果。但若一再地重複進行平面規劃，這是相當耗時的。因此我們利用增量式平面規劃(incremental floorplanning)的觀念，縮短重複進行平面規劃的時間。

在本論文中，我們先取得以任何一種平面規劃(floorplanning)表示法所產生的平面規劃圖，再以Corner Stitching表示法來記錄模組間相對位置關係。為了維持初始平面規劃圖中模組間相對位置關係，我們不重新進平面規劃，取而代之執行一連串增量式運算，包含新增模組與修改模組兩種運算，以得到面積不變與繞線長度較短的平面規劃結果。

實驗結果顯示所提增量式平面規劃演算法確實具有不錯的效能，且在少數模組維度小幅修改時，能產生不錯的平面規劃結果

關鍵詞 : Corner Stitching表示法、平面規劃、增量式平面規劃

目錄

參考文獻

[1]R. H. J. M. Otten (1982)“ Automatic Floorplan Design ” Proceedings of the 19th ACM/IEEE Design Automation Conference, Pages 261-267.
[2]D. F. Wong and C. L. Liu (1986)“ A New Algorithm for Floorplan Designs ” Proceedings of the 23th ACM/IEEE Design Automation Conference, Pages 101-107.
[3]H. Murata, K. Fujiyoshi, S. Nakatake, and Y. Kajitani (1996)“ VLSI Module Placement Based on Rectangle-Packing by the Sequence – Pair ” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 15, Issue 12, Pages 1518-1524.
[4]S. Nakata, K. Fujuoshi, H. Murata, and Y. Kajitani (1996)“ Module Placement Based on BSG-Structure and IC Layout Applications ” Proceedings of the 1996 IEEE/ACM International Conference on Computer-Aided Design, Pages 484-491.
[5]P. N. Guo, C. K. Cheng, and T. Yoshimura (1999)“ An O-tree Representation of Non-Slicing Floorplan and Its Applications ” Proceedings of the 36th ACM/IEEE Design Automation Conference, Pages 268-273.
[6]Y. C. Chang, Y. W. Chang, G. M. Wu, and S. W. Wu (2000)“ B*-Trees: A New Representation for Non-Slicing Floorplans ” Proceedings of the 37th ACM/IEEE Design Automation Conference, Pages 458-463.
[7]X. Hong, G. Huang, Y. Cai, J. Gu, S. Dong, C. K. Cheng, and Jun Gu (2000)“ Corner Block List: An Effective and Efficient Topological Representation of Non-Slicing Floorplan ” Proceedings of the 2000 IEEE/ACM International Conference on Computer-Aided Design, Pages 8-12.
[8]J. M. Lin and Y. W. Chang (2001)“ TCG: A Transitive Closure Graph-Based Representation for Non-Slicing Floorplans ” Proceeding of the 38th ACM/IEEE Design Automation Conference, Pages 764-769.
[9]Peter G. Sassone and Sung K. Lim (2003)“ A Novel Geometric Algorithm for Fast Wire-Optimized Floorplanning ” Proceedings of the 2003 IEEE/ACM International Conference on Computer-Aided Design, Pages 74-80.
[10]Y. Ma, S. Dong, X. Hong, Y. Cai, C. K. Cheng, and J. Gu (2001)“ VLSI Floorplanning with Boundary Constraints Based on Corner Block List ” Proceedings of Asia and South Pacific Design Automation Conference, Pages 509-514.

[11]Y. Ma, X. Hong, S. Dong, Y. Cai, C. K. Cheng, and J. Gu (2001)“A Compact Algorithm for Placement Design Using Corner Block List Representation”Proceedings of the 4th ASIC Conference, Pages 146-149.
[12]X. Tang and D. F. Wong (2002)“Floorplanning with Alignment and Performance Constraints”Proceedings of the 39th ACM/IEEE Design Automation Conference, Pages 848-853.
[13]H. Xiang, X. Tang, and D. F. Wong (2003)“Bus-Driven Floorplanning”Proceedings of the 2003 IEEE/ACM International Conference on Computer-Aided Design, Pages 66-73.
[14]S. Zhou, S. Dong, C. K. Cheng and J. Gu (2001)“ECBL: an extended corner block list with solution space including optimum placement”Proceedings of the 2001 international symposium on Physical design Conference, Pages 150-155.
[15]J. Cong and M. Sarrafzadeh (2000)“Incremental Physical Design”Proceedings of International Symposium on Physical Design, Pages 84-92.
[16]Y. Liu, H. Yang and R. Luo (2003)“An Incremental Floorplanner Based on Genetic Algorithm”Proceedings of 5th International Conference on ASCI Vol.1, Pages 331-334.
[17]L. Yang, Y. Ma, X. Hong, S. Dong and Q. Zhou (2005)“An Incremental Algorithm for Non-Slicing Floorplan Based on Corner Block List Representation”Chinese Journal of Semiconductors Vol.26 No.12, Pages 2335-2343.
[18]Qing. Dong, Bo. Yang, Jing. Li, (2009)“Incremental Buffer Insertion and Module Resizing Algorithm Using Geometric Progra μ ming”Great Lakes Symposium on VLSI, Pages 413-416.
[19]R. A. Finkel and J. L. Bentley (1974)“Quad-tree- a data structure for retrieval oncomposite keys”Acta Informatica, Vol. 4, No.1-9.
[20]N.A. Golias and R.W. Dutton (1997)“Delaunay triangulation and 3D adaptive mesh generation”Finite Elments in Analysis and Design, Vol.25, Pages 331-341.
[21]John K. Ousterfout (1984)“Corner stitching: A data-structuring technique for VLSI layout tools”IEEE Trans.Computer-Aided Design , Pages 87-100.
[22]Chen, Tung-Chieh and Chang (2006)“Modern floorplanning based on B*-tree and fast simulated annealing”Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions onVol.25, Pages 637-650.
[23]高一宏、程仲勝 (2007)“植基於Corner Block List表示法之增量式平面規劃之研究”私立大葉大學電機工程研究所.