

The Implementation of Berlekamp Massey Algorithm Based on Micro-cpu Design

陳建霖、胡大湘

E-mail: 9805522@mail.dyu.edu.tw

ABSTRACT

In this thesis, we devise a micro-cpu, such that Berlekamp-Massey algorithm is performed. A syndrome polynomial computation, an error-location polynomial calculation and its error-location solutions are included. Machine codes are written with iteration structures which can lower the complexity of hardware design. In order to implement Berlekamp-Massey algorithm in a micro-cpu, we design a simple element inversion circuit that performs an inversion in a Galois Field with the least hardware. After simulations are performed correctly by a software ModelSim, a synthesis solution, Synplify Pro-c, is used to synthesize such a micro-cpu circuit. Two kind of error correction capabilities of Berlekamp-Massey algorithm on and are realized, and there is a comparison of cell usage, total Luts, mapping device and so on.

Keywords : Berlekamp-Massey algorithm、Micro-cpu、Element inversion circuit

Table of Contents

封面內頁

簽名頁

授權書	iii
中文摘要	iv
英文摘要	v
誌謝	vi
目錄	vii
圖目錄	ix
表目錄	xi

第一章 緒論

1.1 前言	1
1.2 研究動機	2
1.3 全文架構	2

第二章 Reed-Solomon碼原理

2.1 伽羅瓦場(Galois Field)元素的建立與基本運算	4
2.1.1 伽羅瓦場(Galois Field)基本四則運算	7
2.2 Reed-Solomon碼定義與參數	9
2.3 Reed-Solomon編碼演算法則	10
2.3.1 生成多項式	10
2.3.2 Reed-Solomon編碼演算法則	11
2.4 Reed-Solomon解碼演算法則	13
2.5 Berlekamp-Massey演算法範例	15

第三章 微處理器的架構與運作方式

3.1 微處理器的基本架構	21
3.2 微處理器的基本組成	23
3.3 微處理器的指令擷取方式	24
3.4 微處理器的指令週期的基本概念	25
3.5 微處理器的指令週期	26
3.6 微處理器的指令說明	28

第四章 硬體實現與系統實驗設計

4.1 硬體電路設計	31
4.1.1加法器、乘法器的電路設計	32
4.1.2除法器的電路設計	34
4.1.3特徵值的電路設計	37
4.2 Berlekamp-Massey解碼演算法則結合與驗證	38
4.2.1反元素轉換乘除運算範例	40
4.2.2估算符元錯誤個數	43
4.3 Berlekamp-Massey解碼演算法則實例	45
4.4 Berlekamp-Massey演算法則的電路合成	50

第五章 結論及未來展望

5.1 研究流程與解決問題	55
5.2 結論及未來展望	56

參考文獻	57
----------------	----

REFERENCES

- [1]Jyh-Horng Jeng and Trieu-Kien Truong, “ On Decoding of Both Errors and Erasures of a Reed-Solomon Code Using an Inverse-Free Berlekamp-Massey Algorithm, ” IEEE Transactions on Communications, vol. 47, No. 10, Oct 1999[2]Sergei V. Fedorenko, Member “ A Simple Algorithm for Decoding Reed-Solomon Codes and its Relation to the Welch-Berlekamp Algorithm, ” IEEE Trans.Inf. Theory, vol. 51, no. 3, pp. 2579 – 2587, Sep. 2001.
- [3]Shu Lin, and Daniel J Costello, Jr, “ Error Control Coding, ” Prentice Hall, 2nd edition, 2004[4]李忠昱, “ Implementation of Reed-Solomon Decoder Based on Gao ’ s Algorithm, ” , 大葉大學電信工程學系碩士班碩士論文, 2008[5]William D. Richard, Ph.D., “ Digital Computers I: Organization and Logical Design, ” Nov. 2006. Available: <http://fp.cse.wustl.edu/cse260/>[6] “ Synplify Pro 7.1, ” FPGA Synthesizer with Synplicity, Available: http://www.ee.ccu.edu.tw/~wl/FPGA/Synplify_Pro.pdf[7]劉紹漢、林灶生, “ VHDL晶片設計 , 使用ISE、Modelsim發展系統, ” 全華科技圖書, 台北, 2004。
- [8]唐佩忠, “ VHDL與數位邏輯設計, ” 高立圖書, 2004