# Development of a WiMAX baseband transceiver by using the MIPS-like architecture

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#### **ABSTRACT**

WiMAX is widely applied in mobile wireless communication such as the remote monitoring and the telemedicine service. A lot of the WiMAX chips are embedded with a RISC processor. In this study, a WiMAX baseband transceiver using the RISC MIPS-like architecture in association with the Verilog HDL and ASM is developed. In this work, a WiMAX baseband transceiver designed by C language is compiled and executed with Visual C++ 6 at first. To compile the C program into the MIPS-like machine code by manual operation is too complicated. The C language program is compiled with GCC to generate the MIPS assembly code which can be utilized into PCSpim to carry out PC-based simulation. In addition, the C utility program is developed to fetch the memory content and machine code from PCSpim generated data. The machine code is embedded into the MIPS-like architecture for simulation by using Modelsim with comparison to that by using PCSpim for verification. The MIPS-like architecture embedded with a WiMAX baseband transceiver is synthesized and programmed into FPGA development system interfacing the flash memory by using Xilinx ISE for real signal processing. When the signal process is accomplished, the processed data will appear in flash memory for further verification. All verifications of design flow are accomplished and correct, the MIPS-like architecture can be implemented to achieve VLSI layout automatically under TSMC 0.18 µ m process technology by using Cadence BuildGates and SOC Encounter in wed-based HW/SW co-design framework. The achievement of this work is to develop a WiMAX baseband transceiver by using the MIPS-like architecture. In addition, a C utility program is developed to acquire the memory content and MIPS machine code from the data generated by PCSpim. In association with using the developed utility program, the C design can be rapid prototyped in FPGA chip for verification.

Keywords: WiMAX; MIPS; Verilog HDL; FPGA

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