Web-based HW/SW co-design automation of an 802.16 channel codec

蕭智仁、陳慶順

E-mail: 9804889@mail.dyu.edu.tw

ABSTRACT

This study designs an 802.16 channel codec by using the MIPS-like processor and develops a HW/SW co-design framework in which various EDA tools are effectively integrated. An 802.16 channel codec designed by C program language is compiled with MS Visual C++ 6 to verify its correctness at first. The C design of the 802.16 channel codec is further compiled by GCC compiler to generate the MIPS assembly which can be utilized for MIPS-machine simulation by using PCSpim. The generated machine code by PCSpim can be further embedded into the Verilog behavioral model of the MIPS-like processor. The simulation of Verilog design by ModelSim is with comparison to that by PCSpim for verification. The Virtex-II Pro FPGA development system interfacing with flash memory is applied to verify the aforementioned Verilog model. The Verilog behavioral model is synthesized by using ISE design suite. The data and the program of the 802.16 channel codec are programmed into flash memory, and the synthesized Verilog model of the MIPS-like processor is programmed into FPGA chip, respectively. When the signal encoding or decoding process is accomplished, the encoded or decoded data will appear in flash memory finally for further verification. The web-based HW/SW co-design framework which utilizes Abyss web server, CGI programs, GCC compiler, SPIM simulator, and EDA tools such as Cadence BuildGates and SOC Encounter has been implemented for running in Windows XP and TopologiLinux. In this study, the web-based HW/SW co-design framework can achieve compilation, assembly, simulation, synthesis, and VLSI layout. The main contribution of this study is to develop a web-based HW/SW co-design framework successfully which can design a MIPS-like processor and integrate various EDA tools to achieve VLSI layout automatically. Using the proposed web-based HW/SW co-design automation can reduce the complexity of the design flow.

Keywords : MIPS ; 802.16 channel codec ; web-based ; HW/SW co-design

Table of Contents

REFERENCES

[1] David A. Patterson, John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 3rd ed., Morgan Kaufmann, 2007.

[2] Y. Yao, Q. Yao, P. Liu, Z. Xiao, “ Embedded Software Optimization for MP3 Decoder Implemented on RISC Core, ” IEEE Transactions on Consumer Electronics, vol. 50, pp. 1244-1249, Nov. 2004.

[3] 蔡安朝，陳慶順，潘天賜，“ 實現一個運用似MIPS架構之步進馬達控制系統晶片 ”，2004年中華民國自動控制研討會，大葉大學，2004。

[4] 廖元億，“ 具備非揮發性記憶體介面之可合成似MIPS微處理器結構化模式設計 ”，大葉大學，電機工程學系，碩士論文，2006。

[5] 陳熙儒，“ 運用似MIPS架構實現一個渦輪編碼交錯器 ”，大葉大學，電機工程學系，碩士論文， 2008。

[6] The news from MIPS Technologies, Inc. website, Available: http://www.mips.com/news-events/newsroom/index.cfm?i=1394 [7] A.

Sangiovanni-Vincentelli, The Internet: the next IC design environment, in DAC ’2000 Conference, Keynote presentation, 2000.
[8] V. Nelayev, V. Stempitsky, K. Kudin, “Internet-based IC Technology Design and Simulation,” Proceedings of the 2005 8th Euromicro Conference on Digital System Design. pp. 435-439, Sept. 2005.
[9] IEEE Standard for Local and Metropolitan Area Networks - Part 16: Air Interface for Fixed Broadband Wireless Access Systems, IEEE Std. 802.16-2004, Oct. 2004.
[10] Ambit BuildGates Synthesis User Guide, Cadence Design Systems, Inc., Sep. 2000.
[11] Encounter Menu Reference, Cadence Design Systems, Inc., Jan. 2007.
[12] The GNU Compiler Collection, Free Software Foundation, Inc., Available: http://gcc.gnu.org/ [13] James R. Larus, SPIM: A MIPS32 Simulation, Available: http://pages.cs.wisc.edu/~larus/spim.html [14] Mark G. Arnold, Verilog Digital Computer Design: Algorithms into Hardware, Prentice-Hall, Inc., 1999.
[15] ModelSim User ’s Manual, Mentor Graphics Corp., Available: http://www.model.com/resources/resources_manuals.asp [16] Thomas Boutell, CGI Programming in C and Perl, Addison-Wesley Professional, 1996.
[17] Jeffrey G. Andrews, Arunabha Ghosh, Rias Muhamed, Fundamentals of WiMAX: Understanding Broadband Wireless Networking, Prentice-Hall, Feb. 2007.
[18] ISE In-Depth Tutorial, Xilinx, Inc., Available: http://download.xilinx.com/direct/ise8_tutorials/ise8tut.pdf [19] MIPS32TM Architecture For Programmers Volume II: The MIPS32 Instruction Set, MIPS Technologies Inc., Jul. 2005.
[20] W29C011A - 128K × 8 CMOS FLASH MEMORY, Winbond Electronics Corp., Jan. 2002. Available: http://www.datasheetsite.com/datasheet/W29C011A [21] Hardware reference manual of the Virtex-II Pro Development System, Xilinx, Inc., Mar. 2005. Available: http://www.digilentinc.com/Data/Products/XUPV2P/XUPV2P_User_Guide.pdf [22] 張弘琦，“以0.18μm CMOS積體電路技術設計支援大部份MIPS指令的低分支代價處理器”，台灣大學，電子工程學研究所，碩士論文，2005。