

# Implementation of a JPEG Encoding System on Chip Using the MIPS-like Architecture

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## ABSTRACT

JPEG encoding is widely applied in present 3C products such as digital camera and mobile phone. This study develops a 32-bits RISC (Reduced Instruction Set Computer) microprocessor with the MIPS-like architecture embedded a JPEG encoder by using the Verilog HDL (Hardware Description Language) and ASM (Algorithmic State Machine). A JPEG encoder designed by C program language is compiled with MS Visual C++ 6 to verify its correctness at first. The C design of the JPEG encoder is further compiled by GCC compiler to generate the MIPS assembly which can be utilized for MIPS-machine simulation and machine code extraction by using PCSPim. The relative machine code can be embedded into the Verilog behavioral model of a MIPS-like processor. The HW/SW co-design with using Verilog can be simulated by ModelSim and the simulation result is with comparison to that by PCSPim. The Virtex-II Pro (V2-Pro) FPGA development system interfacing with flash memory is applied to verify the aforementioned Verilog model. The behavioral Verilog model is synthesized and programmed into the FPGA board by using ISE design suite. The image data and the JPEG encoder program are programmed into flash memory, and the synthesized Verilog model of the MIPS-like microprocessor is programmed into FPGA chip, respectively. When the JPEG encoding is accomplished, the coded data of the image will appear in flash memory finally for further verification. In addition, the Verilog structure model of a MIPS-like microprocessor can be automatically generated by using Cadence BuildGates. The synthesized netlist from BuildGates is further imported to Cadence SOC Encounter for VLSI layout with using TSMC 90nm standard cell library. The objective of this work is to develop a HW/SW co-design framework which can effectively integrate various EDA tools. The developed C design which may be resulted from various research fields such as digital control, multimedia technology, and digital communication, can be rapid prototyped in FPGA chip for verification and implemented in VLSI layout.

Keywords : Verilog HDL、JPEG、MIPS、FPGA

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