Two-Layer Floorplanning Based on Sequence-Pair Representation

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ABSTRACT

Floorplanning is a very important step of physical design in the backend of IC design. Generally, one layer floorplanning problem is to solve the problem of placement on 2D plane. However, as system chip becomes more complex, System-On-a-Chip (SoC) becomes growing up, some modules of system must be placed on different layers to decrease the complexity of design and fabrication, the problem of 3D floorplanning is hence derived. In this work, two-layer floorplanning is considered, that is, modules can be placed on any one of both layers. Each layer has its own width, height, and area after placement, and chip could be formed by vertically combining both layers. The objective is to find the minimum chip area and total wire length. In our method, modules are first partitioned into two groups by different partition strategies, then Sequence-Pair floorplanning algorithm and simulated annealing procedure are used to obtain optimal solution for each layer. Finally, two layers are combined to form the whole chip.

Keywords : physical design ; floorplanning

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