

植基於Sequence-Pair表示法之雙層平面規劃之研究 = Two-layer floorplanning based on sequence-pair representation

孫文彥、程仲勝

E-mail: 9708437@mail.dyu.edu.tw

摘要

積體電路後端實體設計(physical design)中，平面規劃(floorplanning)一直是一個相當重要的設計步驟。一般單層平面規劃問題即是解決模組在2D平面上之擺放問題；然而隨著系統晶片複雜度的提高，System-On-a-Chip (SoC)的系統設計日趨成熟，有些系統之模組必須擺放在不同層以降低設計及製造之複雜度，因此衍生出3D平面規劃的問題。本論文中我們考慮雙層平面規劃問題，亦即將模組擺放在上下兩層2D平面，每層各有其模組擺放後之寬、高及面積，上下兩層垂直結合後可形成整個晶片，而目標則為尋找最小之晶片面積及繞線總長度。我們嘗試以不同的策略將模組分為兩堆，每堆模組擺放在同一層，而每層分別使用Sequence-Pair平面規劃演算法[4]及模擬退火(simulated annealing)程序找出最佳解，最後再將兩層上下結合以求出最終晶片。

關鍵詞：實體設計；平面規劃

目錄

封面內頁 簽名頁 授權	iii	中文摘要	
	iv	英文摘要	v
	vi	目錄	vii
	x	表目錄	xv
第一章 緒論	1	1.1 研究背景與動機	
1.1.2 研究方法	1	1.1.3 論文架構	
第二章 平面規劃相關研究	3	2.1 一般平面規劃問題描述	
2.2 可切割平面規劃表示法	4	2.2.1 Shorthand Tree	
2.2.2 Normalized Polish Expression	4	2.3 不可切割平面規劃表示法	
2.3.1 Sequence-Pair表示法	6	2.3.2 Bounded-Sliceline Grid表示法	
2.3.3 Corner Block List表示法	8	2.3.4 O-tree表示法	
2.3.5 B*-tree 表示法	10	2.3.6 Transitive Closure Graph表示法	12
2.3.7 梯形平面規劃器	14	2.4 3D平面規劃	15
第三章 以Sequence-Pair表示法進行雙層平面規劃	17	3.1 問題描述	
3.2 雙層平面規劃演算法	17	3.3 模組分堆方法	
3.3.1 方法一：隨機將模組分堆	19	3.3.2 方法二：等面積將模組分堆	
3.3.3 方法三：使用計算權重值方法	21	3.4 雙層平面規劃結合	
3.5 雙層平面規劃繞線估計	29	3.5.1 半週長估計方式	
3.5.2 繞線長度估計	31	3.5.3 判斷矩形是否重疊之計算方法	35
3.6 雙層模組交換進行模擬退火	37	第四章 實驗結果	
4.1 使用三種不同分堆方法	38	4.2 模組群聚	
4.3 限制各層面積的寬高比例(aspect ratio)	43	第五章 結論與未來展望	
參考文獻	57	附錄A n100測試電路實驗結果	
A-1 A.1 使用三種不同分堆方法		A-1 A.2 模組群聚	
A-5 A.3 限制各層面積的寬高比例(aspect ratio)		附錄B n200測試電路實驗結果	
B-1 B.1 使用三種不同分堆方法		B-1 B.2 模組群聚	
B-5 B.3 限制各層面積的寬高比例(aspect ratio)		附錄C n600測試電路實驗結果	
C-1 C.1 使用三種不同分堆方法		C-1 C.2 模組群聚	
C-6 C.3 限制各層面積的寬高比例(aspect ratio)			C-17

參考文獻

- [1] R. H. J. M. Otten (1982) "Automatic Floorplan Design" Proceedings of 19th ACM/IEEE Design Automation Conference, Pages 261 – 267.
- [2] D. F. Wong and C. L. Liu (1986) "A New Algorithm for Floorplan Designs" Proceedings of 23rd ACM/IEEE Design Automation Conference, Pages 101 – 107.
- [3] H. Onodera, Y. Taniguchi, and K. Tamaru (1991) "Branch-and-Bound Placement for Building Block Layout" Proceedings of 28rd ACM/IEEE Design Automation Conference, Pages 433 – 439.
- [4] H. Murata, K. Fujiyoshi, S. Nakatake, and Y. Kajitani (1996) "VLSI Module Placement Based on Rectangle-Packing by the Sequence – Pair" Proceedings of IEEE Transaction on Computer Aided Design of Integrated Circuits and System, Volume 15, Issue 2, Pages 1518 – 1524.
- [5] S. Nakata, K. Fujiyoshi, H. Murata, and Y. Kajitani (1996) "Module Placement on BSG-Structure and IC Layout Applications" Proceedings of the 1996 IEEE/ACM International Conference on Computer-Aided Design, Pages 484 – 491.
- [6] J. Xu, P. N. Guo, and C. K. Cheng (1998) "Rectilinear Block Placement Using Sequence-Pair" Proceedings of the 1998 International Symposium on Physical Design, Pages 173 – 178.
- [7] P. N. Guo, C. K. Cheng, and T. Yoshimura (1999) "An O-tree Representation of Non-Slicing Floorplan, and Its Applications" Proceedings of the 36th ACM/IEEE Design Automation Conference, Pages 268 – 273.
- [8] K. Bazargan, S. Kim, and M. Sarrafzadeh (1999) "Nostradamus: A Floorplanner of Uncertain Designs" IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, Volume 18, Issue 4, Pages 389 – 397.
- [9] Y. C. Chang, Y.W. Chang, G. M. Wu, and S. W. Wu (2000) "B*-Trees: A New Representation for Non-Slicing Floorplans" Proceedings of the 37th Design Automation Conference, Pages 458 – 463.
- [10] X. Hong, G. Huang, Y. Cai, J. Gu, S. Dong, C. K. Cheng, and J. Gu (2000) "Corner Block List: An Effective and Efficient Topological Representation of Non-Slicing Floorplan" Proceedings of the 2000 IEEE/ACM International Conference on Computer-Aided Design, Pages 8 – 12.
- [11] J. M. Lin and Y. W. Chang (2001) "TCG: A Transitive Closure Graph-Based Representation for Non-Slicing Floorplans" Proceeding of 38th Design Automation Conference, Pages 764 – 769.
- [12] X. Tang, R. Tian, and D. F. Wong (2001) "Fast Evaluation of Sequence Pair in Block Placement by Longest Common Subsequence Computation" IEEE Transaction on Computer Aided Design of Integrated Circuits and System, Volume 20, Issue 12, Pages 1406 – 1413.
- [13] Y. Deng, W. Maly(2001) "Interconnect Characteristics of 2.5-D System Integration Scheme", Proceedings of Symposium on Physical Design, Pages 171-175.
- [14] X. Tang and D. F. Wong (2002) "Floorplanning with Alignment and Performance Constraints" Proceedings of 39th Design Automation Conference, Pages 848 – 853.
- [15] K. Sakanushi, Y. Kajitani, and D.P. Mehta (2003) "The Quarter-State-Sequence Floorplan Representation" Proceedings of IEEE Transaction on Circuits and Systems – I: Fundamental Theory and Applications, Volume 50, Issue 3, Pages 376 – 386.
- [16] H. Xiang, X. Tang, and D. F. Wong (2003) "Bus-Driven Floorplanning" Proceedings of the 2003 IEEE/ACM International Conference on Computer-Aided Design, Pages 66 – 73.
- [17] P. G. Sassone and S. K. Lim (2003) "A Novel Geometric Algorithm for Fast Wire-Optimized Floorplanning" Proceedings of the 2003 IEEE/ACM International Conference on Computer-Aided Design, Pages 74-80.
- [18] S. Das, A. Chandrakasan, and R. Reif(2003) "Design Tools for 3-D Integrated Circuits". Proceedings of Asia South Pacific Design Automation Conference, Pages 53-56.
- [19] J. Li, T. Yan, B. Yang, J. Yu, and C. Li (2004) "A Packing Algorithm for Non-Manhattan Hexagon/Triangle Placement Design by Using An Adaptive O-Tree Representation" Proceeding of 41st Design Automation Conference, Pages 646 – 651 .
- [20] J. Cong, J. Wei, and Y. Zhang (2004) "A Thermal-Driven Floorplanning Algorithm for 3D ICs" Proceedings of the 2004 IEEE/ACM International Conference on Computer-Aided Design, Pages 306 – 313.
- [21] J. Cong, G. Luo, J. Wei, Y. Zhang(2007) "Thermal-Aware 3D IC Placement Via Transformation". 12th Asia and South Pacific Design Automation Conference (ASPDAC2007), Pages 780-785.
- [22] 吳彬玄、習存榮、程仲勝 (2003), "考慮電磁相容之超大型積體電路平面規劃之研究" Proceedings of the 2003 Taiwan Electromagnetic Compatibility Conference, Pages 78-83.
- [23] 高一宏、潘佳信、孫文彥、程仲勝 (2006), "以限制閒置空間大小的群聚策略解決平面規劃問題" Proceedings of Applications of Information, Management and Communication Technology Symposium.