Noise-Aware Power Optimization Technique for MTCMOS Circuits

許堅致、林浩仁

E-mail: 9708329@mail.dyu.edu.tw

ABSTRACT

Subthreshold leakage current and crosstalk noise are two important issues of integrated circuits in nanometer technology node. MTCMOS (Multi-Threshold CMOS) is a technology that allows the devices in a circuit to be with different threshold voltages (VTH). It is used to assign the devices on the timing critical path with low VTH to preserve the high performance and assign the devices on the non-critical path with high VTH to reduce the leakage. This is an effective way to achieve high performance and low power goal by adequately assigning the threshold voltage of each device in a circuit. In this paper, we take the above mentioned two issues into consideration. With considering the crosstalk and leakage issues simultaneously, we have the following observation. If the input signal of a device on the critical path has the crosstalk noise problem, then the device should be assigned with high VTH since high VTH device is less sensitive to noise. We propose an algorithm based on the above observation. We first extract the coupling capacitances of aggressor and victim nets from the standard-cell-based layout of a circuit. Then, crosstalk noise analysis is performed to find out the nets with larger noise which is measured by the "maximum peak voltage". The second step is to identify the critical path. By the results of the above steps, we globally assign each cell with either high-Vth or low-Vth version from the cell library to achieve the noise-aware and low-power design goal. Experiments are performed on the circuits from the ISCAS89 benchmark suite. First, the circuit is implemented using the TSMC 0.13um dual threshold standard-cell library. Then, the commercial tool SOC Encounter is used to perform the placement and routing work and crosstalk analysis of the circuit. After applying our proposed algorithm, we can reduce the number of nets with noise greater then VDD*10% about 17%.

Keywords : Low-Power ; Design ; Leakage ; MTCMOS ; Crosstalk noise

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REFERENCES

[1] Magma Design Automation "Signal Integrity Sign-off Verification", White Paper, 2002.

[2] C. Chen, X. Yang, M. Sarrafzadeh. "Potential Slack: An Effective Metric of Combinational Circuit Performance. In Proc. of the ACM/IEEE International Conference on Computer-Aided Design, pp. 198-201, 2000.

[3] Chou, H, and S Chiu, "Crosstalk Reduction and Tolerance in Deep Sub-Micron Interconnects", Technical Report, Department of Electrical and Computer Engineering, University of Wisconsin, Madison, 2001.

[4] Dubey, S, and Jorgenson J, "Crosstalk reduction using buffer insertion," In Proc. of the IEEE International Symposium on Electromagnetic Compatibility, pp. 639-642, 2002.

[5] T. Zhang and S. S. Sapatnekar, "Simultaneous Shield and Buffer Insertion for Crosstalk Noise Reduction in Global Routing," In Proc. of the IEEE International Conference on Computer Design, pp. 93 – 98, 2004.

[6] C. J. Alpert, J. Hu, S. S. Sapatnekar and P. Villarrubia, "A Practical Methodology for Early Buffer and Wire Resource Allocation," In Proc. of the ACM/IEEE Design Automation Conference, pp. 189 – 194, 2001.

[7] C.J. Alpert, A. Devgan and S.T. Quay, "Buffer insertion for noise and delay optimization," IEEE Trans. Computer-Aided Design Integrated Circuits and Systems 18 11, pp. 1633 – 1645 1999.

[8] A. Vittal, M. Marek-Sadowska, "Crosstalk Reduction for VLSI," IEEE. Trans. Computer-Aided Design, vol. 16, pp. 290-298, Mar. 1997.
[9] J. Cong, D. Pan, and P. V. Srinivas, "Improved crosstalk modeling for noise constrained interconnect optimization", in Proc. Asia South Pacific Design Automation Conf., 2001, pp. 373 – 378 [10] Qingjian Yu; Kuh, E.S.; New efficient and accurate moment matching based model for crosstalk estimation in coupled RC trees," IEEE, Quality Electronic Design, 2001, pp. 151 – 157.

[11] Xiaoliang Bai, Chandra R., Dey, S., Srinivas P.V., "Interconnect coupling-aware driver modeling in static noise analysis for nanometer circuits", Computer-Aided Design of Integrated Circuits and Systems, vol. 23, 2004, pp. 1256 – 1263.

[12] L. Wei, Z. Chen, M. Johnson, and K. Roy, "Design and Optimization of Low Voltage High Performance Dual Threshold CMOS Circuits, "in Proc. of DAC, June 1998, Page(s): 489-492.

[13] M. Ketkar, S.S. Sapatnekar, "Standby power optimization via transistor sizing and dual threshold voltage assignment," in Proc. of ICCAD, Nov. 2002, Page(s): 375 - 378.

[14] Jeegar Tilak Shah, Marius Evers, Jeff Trull, Alper Halbutogullari, "Circuit optimization for leakage power reduction using multi-threshold voltages for high performance microprocessors." ISPD 2007: 67-74 [15] Chuhong Chen, X. Yang and Majid Sarrafzadeh, "Potential Slack: An Effective Metric of Combinational Circuit Performance," Proceedings of ICCAD,pp.198-201, 2000.

[16] Yen-Te Ho, Ting-Ting Hwang, Low power design using dual threshold voltage, Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair, p.205-208, January 27-30, 2004, Yokohama, Japan [17] Kanak Agarwal, Dennis Sylvester, David Blaauw, "Modeling and Analysis of Crosstalk Noise in Coupled RLC Interconnects," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T-CAD), Vol. 25, No. 5, May 2006, pg. 892-901, short paper [18] Seong-Ook Jung, Ki-Wook Kim, Sung-Mo Kang. "Noise constrained transistor sizing and power optimization for dual Vt domino logic "Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 10, Issue 5, Oct. 2002 Page(s):532 – 541 [19] Anis, M.H, Allam, M.W, Elmasry, M.I, "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies "Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 10, Issue 2, April 2002 Page(s):71 – 78 [20] Seong-Ook Jung, Ki-Wook Kim, Sung-Mo Kang, "Dual threshold voltage domino logic synthesis for high performance with noise and power constraint "Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings 4-8 March 2002 Page(s):260 – 265 [21] Seong-Ook Jung, Ki-Wook Kim, Sung-Mo Kang, "Noise constrained power optimization for dual VT domino logic "Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on Volume 4, 6-9 May 2001 Page(s):158 - 161 vol. 4 [22] B. Young, "Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages", Prentice Hall, 2001.