雜訊限制的MTCMOS電路供率優化方法之設計 = Noise-aware power optimization technique for MTCMOS circuits

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摘 要

漏電流(Leakage)與耦合雜訊(Crosstalk)是目前奈米世代積體電路設計的重要課題，對於漏電流的處理，由於Multiple Threshold Voltages CMOS(MTCMOS)製程技術不會增加電路設計的複雜度，是近年來相當受到重視的方法。目前MTCMOS電路的Vth值選用策略為：將關鍵路徑(Critical path)上的邏輯元件以Low-Vth的樣式實現，以維持電路的效能(Performance)；而非關鍵路徑上的元件則採用High-Vth樣式，以降低漏電流。 本篇論文針對MTCMOS電路，加入考量雜訊影響的觀點，由於Low-Vth元件的雜訊免疫力比High-Vth元件差，因此在佈局中雜訊較敏感區域中的元件，應該盡量以High-Vth的樣式實現，以提高電路的強健性(Robustness)與可靠性(Reliability)。但是若這些元件也是在關鍵路徑上，則會與前述效能的原則而採用Low-Vth樣式互相牴觸。基於前述的觀察與發現，本論文提出：在關鍵路徑上且耦合雜訊嚴重區域的邏輯元件，應該採用High-Vth樣式，而非Low-Vth樣式，以避免較嚴重的耦合雜訊造成邏輯元件的功能錯誤。以前述的觀點為核心，本論文提出考量雜訊的MTCMOS電路元件VTH值選擇演算法。以ISCAS89測試電路進行實驗，在不增加電路時間延遲的限制下，本論文所設計的演算法平均可將耦合雜訊值大於VDD*10%的連接線數目降低17%。

關鍵詞 : 低功率設計 ; 漏電流 ; MTCMOS ; 耦合雜訊干擾

目錄

參考文獻

[1] Magma Design Automation “ Signal Integrity Sign-off Verification ”, White Paper, 2002.

[2] C. Chen, X. Yang, M. Sarrafzadeh. "Potential Slack: An Effective Metric of Combinational Circuit Performance. In Proc. of the ACM/IEEE International Conference on Computer-Aided Design, pp. 198-201, 2000.

[3] Chou, H, and S Chiu, “ Crosstalk Reduction and Tolerance in Deep Sub-Micron Interconnects ”, Technical Report, Department of Electrical and Computer Engineering, University of Wisconsin, Madison, 2001.

[4] Dubey, S, and Jorgenson J, “ Crosstalk reduction using buffer insertion, ” In Proc. of the IEEE International Symposium on Electromagnetic Compatibility, pp. 639-642, 2002.

[5] T. Zhang and S. S. Sapatnekar, “ Simultaneous Shield and Buffer Insertion for Crosstalk Noise Reduction in Global Routing, ” In Proc. of the IEEE International Conference on Computer Design, pp. 93 – 98, 2004.

[6] C. J. Alpert, J. Hu, S. S. Sapatnekar and P. Villarrubia, “ A Practical Methodology for Early Buffer and Wire Resource Allocation, ” In Proc. of the ACM/IEEE Design Automation Conference, pp. 189 – 194, 2001.

[7] C.J. Alpert, A. Devgan and S.T. Quay, “ Buffer insertion for noise and delay optimization, ” IEEE Trans. Computer-Aided Design Integrated Circuits and Systems 18 11, pp. 1633 – 1645 1999.

[8] A. Vittal, M. Marek-Sadowska, “ Crosstalk Reduction for VLSI, ” IEEE. Trans. Computer-Aided Design, vol. 16, pp. 290-298, Mar. 1997.

[9] J. Cong, D. Pan, and P. V. Srinivas, “ Improved crosstalk modeling for noise constrained interconnect optimization ”,in Proc. Asia South Pacific Design Automation Conf., 2001, pp. 373 – 378 [10] Qingjian Yu; Kuh, E.S.; ” New efficient and accurate moment matching based model for crosstalk estimation in coupled RC trees, ” IEEE ,Quality Electronic Design, 2001, pp. 151 – 157.

[11] Xiaoliang Bai, Chandra R.,Dey, S. ,Srinivas P.V. , “ Interconnect coupling-aware driver modeling in static noise analysis for nanometer circuits ”, Computer-Aided Design of Integrated Circuits and Systems, vol. 23, 2004, pp. 1256 – 1263.

[12] L. Wei, Z. Chen, M. Johnson, and K. Roy, “ Design and Optimization of Low Voltage High Performance Dual Threshold CMOS Circuits, ” in Proc. of DAC, June 1998, Page(s): 489-492.

[13] M. Ketkar, S.S. Sapatnekar, “ Standby power optimization via transistor sizing and dual threshold voltage assignment, ” in Proc. of ICCAD, Nov. 2002, Page(s): 375 -378.
[14] Jeegar Tilak Shah, Marius Evers, Jeff Trull, Alper Halbutogullari, ” Circuit optimization for leakage power reduction using multi-threshold voltages for high performance microprocessors. ” ISPD 2007: 67-74 [15] Chuhong Chen, X. Yang and Majid Sarrafzadeh, ” Potential Slack: An Effective Metric of Combinational Circuit Performance, ” Proceedings of ICCAD,pp.198-201, 2000.
[16] Yen-Te Ho , Ting-Ting Hwang, Low power design using dual threshold voltage, Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair, p.205-208, January 27-30, 2004, Yokohama, Japan [17] Kanak Agarwal, Dennis Sylvester, David Blaauw, "Modeling and Analysis of Crosstalk Noise in Coupled RLC Interconnects," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T-CAD), Vol. 25, No. 5, May 2006, pg. 892-901, short paper [18] Seong-Ook Jung, Ki-Wook Kim, Sung-Mo Kang. ” Noise constrained transistor sizing and power optimization for dual Vt domino logic ” Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 10, Issue 5, Oct. 2002 Page(s):532 – 541 [19] Anis, M.H, Allam, M.W, Elmasry, M.I, “ Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies ” Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 10, Issue 2, April 2002 Page(s):71 – 78 [20] Seong-Ook Jung, Ki-Wook Kim, Sung-Mo Kang, ” Dual threshold voltage domino logic synthesis for high performance with noise and power constraint ” Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings 4-8 March 2002 Page(s):260 – 265 [21] Seong-Ook Jung, Ki-Wook Kim, Sung-Mo Kang, ” Noise constrained power optimization for dual VT domino logic “ Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on Volume 4, 6-9 May 2001 Page(s):158 - 161 vol. 4 [22] B. Young, “ Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages ”, Prentice Hall, 2001.