Exploiting Cache Design Space Variation under the Influence of Compiler Optimization Options：A Case Study of H.264

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ABSTRACT

Merging of mobile computing and multimedia application opens many new opportunities for industry of information technology and benefits our daily life. However the merge also brings new technical challenges to computer designers. Among the others, power consumption has being a major concerned. The high data accessing rate of multimedia applications consume a great percentage of overall battery power of mobile device. This thesis studies variation of cache performance, cost, and power consumption that under different compiler optimization options. The ITU H.264 has being adapted in this study for its prevalence. The most frequent function of the ITU H.264 reference design is extracted by using profiling techniques. The extracted function is then compiled under different optimization options that generate a set of testbench programs. These testbenches are simulated under Sim-Panalyzer that a StrongARM simulator equipped with power simulation capability. The simulation shows program optimization not only increase the performance but also decrease overall power consumption of the CPU.

Keywords : StrongARM ; H.264 ; Sim-Panalyzer ; power consumption ; performance

Table of Contents

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