The Implementation of Feng-Tzeng Algorithm

E-mail: 9707286@ mail.dyu.edu.tw

ABSTRACT

The Reed-Solomon (RS) ode is a kind of powerful error control code, which can correct burst errors and the random errors. RS codes have been applied in many systems. The Feng-Tzeng algorithm is an extension of the Berlekamp-Massey, and it is used to decode RS codes. This algorithm can produce a shortest polynomial linearly dependent on a given matrix. In this thesis, the Feng-Tzeng algorithm is realized with VHDL, which is downloaded the Xilinx VirtexII embedded system for verification. Firstly, a codeword of an RS code is generated and interfered by random noises and then sent into an embedded system via an RS232 interface in a personal computer. After the Feng-Tzeng decoder, which is the hardware of Feng-Tzeng decoding, has performed, the decoded sequence is sent back in order to compare the original data and verify if the performance of this Feng-Tzeng decoder is exact or not.

Keywords : Reed-Solomon code ; Feng-Tzeng Alogrithm

Table of Contents

REFERENCES

[1]Gui-Liang Feng and Kenneth K.Tzeng " A Generalization of the Berlekamp-Massey Alogrithm for Multisequence Shift-Register Synthesis with Applications to Decoding Cyclic Code" IEEE Transactions Information Theory,VOL.37,NO.5.SEPTEMBER 1991 , pp.1274-1286
[2]S.Lin and D.J. Costello, Jr, " Error Control Coding", 2nd edition Prentice Hall, 2004 [3]Nicola Petra,Davide De Caro Antonio G.M Strollo
" A Novel Architecture for Galois Fields Multipliers Based on Mastrovito Scheme" IEEE Transactions On Computers
    VOL.56,NO.11,NOVEMBER 2007,pp1470-1475 [4]   ,"   "
        ,2007 [5]   " A Low-complexity VLSI architecture of the Reed-Solomon codec"   ,2001 [6]   ,"
                                    " ,   ,2003 [7]   ,"
        " ,   ,2005 [8]   ,"   "
            ,2007 [9]   " VHDL   "   ,2004 [10]   .   "   VHDL
    ISE   MODELSIM   "   ,2005 [11]   " FPGA   BCH code
        "   ,2006