

# The Implementation of Low - Density Parity - Check Decoding

賴偉誌、胡大湘

E-mail: 9707283@mail.dyu.edu.tw

## ABSTRACT

The error control coding is different from the source coding in general. In the transmission, the data are degraded by unreliable transmit media or interfered with the external factor, the error control coding is employed to correct errors as much as possible. Low density parity check (LDPC) code is a kind of powerful error control coding. Data encoded with LDPC code are sent with lower power and then could be received correctly with LDPC decoder employed. In this thesis, the sum-product algorithm of LDPC code is implemented by VHDL, which employs some mathematical functions and float-point calculation packages. Over a noisy simulation transmission channel, interfered data are detected in such a decoding algorithm and then decoded. The results of C language simulation and VHDL language simulation are compared. The implementation of this algorithm is downloaded to an FPGA development system. Such an implementation in FPGA has been verified to correct interfered data, and then these corrected data are sent back to a personal computer via RS232 interface

Keywords : LDPC code ; Hyperbolic ; Error control coding ; SPA algorithm

## Table of Contents

封面內頁 簽名頁 授權書 . . . . .	iii	中文摘要 . . . . .	iii
. . . . . iv 英文摘要 . . . . .	iv	v 誌謝 . . . . .	v
. . . . . vi 目錄 . . . . .	vi	vii 圖目錄 . . . . .	vii
. . . . . ix 表目錄 . . . . .	ix	xi 第 . . . . .	xi
第一章 緒論 1.1 前言 . . . . .	1	1.2 錯誤更正碼 . . . . .	1
1.3 研究動機 . . . . .	2	第二章 低密度奇偶校驗碼原理 2.1 低密度奇偶校驗碼簡介 . . . . .	2
. . . . . 3 2.2 有限場 . . . . .	3	2.3 低密度奇偶校驗碼之編碼 . . . . .	3
. . . . . 4 2.3.1 生成多項式 . . . . .	5	2.3.2 Parity-Check Matrix of LDPC Code . . . . .	6
編碼範例 . . . . .	11	第三章 低密度奇偶校驗碼之解碼 3.1 The Sum-Product	Algorithm . . . . .
Algorithm . . . . .	14	3.1.1 計算所有非本質 . . . . .	15
. . . . . 17	17	3.1.2 錯誤更正 . . . . .	17
. . . . . 21	21	3.1.3 錯誤檢測與驗證 . . . . .	18
第四章 實現模擬與驗證 4.1 設計流程 . . . . .	29	3.2 解碼範例 . . . . .	18
電路實現與模擬 . . . . .	31	4.2 編碼器	電路實現與模擬 . . . . .
. . . . . 34	34	4.3 解碼器電路實現與模擬 . . . . .	33
. . . . . 48	48	4.3.1 CORDIC 演	算器 . . . . .
. . . . . 59	59	4.3.2 CORDIC演算器電路架構 . . . . .	40
		4.3.3 指數函數的實現 . . . . .	
		4.4 模擬結果驗證與比對 . . . . .	51
		第五章 結論及未來展望 參考文獻 . . . . .	

## REFERENCES

- [1] S. Lin and D. J. Costello, Jr, " Error Control Coding ", 2nd edition Prentice Hall, 2004, pp.309-311 [2] 施忠賢, " A Novel Hybrid CORDIC Algorithm with A Variable Scalar Factor for Sine and Cosine Computation ", 逢甲大學 資訊工程研究所碩士論文, 1999 [3] 黃朝全, " CORDIC-Based Signed-bit Predictable SIN-COS Generator And It ' s FPGA Implementation ", 中山大學 資訊工程研究所碩士論文, 2000 [4] 柏堂宏, " CORDIC Algorithm and Architecture ", 台灣大學 電機工程學系 VLSI Signal Processing Final Report, 2000 [5] 林凱立, " High-Throughput Low-Density Parity-Check Code Decoder Designs ", 交通大學 電子工程學系 電子研究所碩士班碩士論文, 2005 [6] 林永哲, " A Study on LDPC Coding Technique and Its Application to Digital Video Broadcasting Systems ", 交通大學 電信工程學系碩士班碩士論文, 2005 [7] 江佳陽, " Low Density Parity Check Code and Density Evolution ", 中正大學 通訊工程研究所碩士論文, 2006 [8] 蔡坤均, " Message Passing Algorithms on Generator Matrices ", 中正大學 通訊工程研究所碩士論文, 2006 [9] 鄭佳瑋, " Design and Implementation of High-Throughput LDPC Decoder for IEEE 802.3an Applications ", 交通大學 電子工程學系 電子研究所碩士論文, 2006 [10] 劉紹漢、林灶生, 最新VHDL晶片設計使用ISE、MODELSIM發展系統, 全華科技圖書, 2005 [11] <http://www.eda.org/vhdl-200x/vhdl-200x-ft/packages/files.html>, VHDL-2006 packages [12] 陳乃塘, " LDPC性能激發高度需求依應用領域選擇合適錯誤控制碼 ", 新通訊, 2005