Implementation of an Interleaver for Turbo Codes Using the MIPS-like Architecture

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ABSTRACT

The turbo codes are wildly applied in most leading technology of wireless communication. Therefore, this study develops a 32-bit RISC (Reduced Instruction Set Computer) microprocessor with the MIPS-like architecture embedded an interleaver for turbo codes by using the Verilog HDL (Hardware Description Language) and ASM (Algorithmic State Machine). In this work, the interleaver for turbo codes is designed by C language at first. Furthermore, the design is compiled with LCC (Little C Compiler) to generate the assembly code. The C utility program developed by our research group is applied to modify the assembly code. The modified assembly code can be utilized into PCSpim to carry out the PC-based simulation and machine code. The machine code generated by PCSpim is embedded into the MIPS-like core for digital simulation by using ModelSim with comparison to previous simulation by using PCSpim for verification. In addition, the whole design is further synthesized by using Xilinx FPGA development software. The VLSI layout of the microprocessor embedded an interleaver for turbo codes is implemented under TSMC 0.18 um process technology at final. The result of this study is applicable to the turbo-code encoder of CDMA IS-2000 system, and we expect the study is able to be extended to the design of turbo-code encoder and decoder, WiMAX and MPSOC in the near future.

Keywords : Turbo Cording , Verilog , FPGA , MIPS , System-on-a-Chip

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