Multi-Layer PCB Ground Planes Topology and Bounce Noise Suppressing

張永祥、胡永栴

E-mail: 9706060@mail.dyu.edu.tw

ABSTRACT

This thesis presents the Multi-Layer PCB Ground Planes Topology and Bounce Noise suppressing theory which motive study and research on chapter 1, chapter 2 is the grounding bounce of the miscellaneous signal to detail (Ground Bounce Noise) Formulation and the circulation way, and it is the current to analyse and can not solve by method of this kind problems. Prove with PCB open up Topology Trace Layout circuit board make and compare at present by naked circuit in chapter 3, survey with simulation result is it suppress grounding bounce miscellaneous result of new way to prove relatively, propose some pluses and minuses are compared. Chapter 4 compare result of the numerical simulation with experiment, test simulation procedure open up topology geometry influence of structure on all kinds of it and then discuss the implicit physics meaning of all groups of data. Chapter 5 put the method of resisting the miscellaneous new spreading in order, discussion open up topology structure method and difference and pluses and minuses of traditional method at present, do it into a conclusion. Thesis this put in order multi-layer printed circuit board resistance miscellaneous method and ground that new travel open up structure topology with bounce miscellaneous signal suppress finally difference of new method and traditional method.

Keywords : Grounding bounce miscellaneous、circuit board、open up topology geometry structure、resistance of the miscellaneous signal.

Table of Contents

REFERENCES

[1] Mark I. Montrose, EMC and the Printed Circuit Board. Piscataway, NJ:IEEE Press, 1998.

[2] Mark I. Montrose, Printed Circuit Board Design Techniques for EMC Compliance. Piscataway, NJ:IEEE Press, 1996.

[3] Kumaresh Bathey, Madhavan Swaminathan, L. D. Smith, T. J. Cockerill, "Noise Computation in Single Chip Packages," IEEE Trans. Comp., Packag., Maunfact., Technol., pp.350-358, May 1996.

[4] Takashi Harada, et al., "Radiated Emission Arising from Power Distribution in Multi-layer Printed Circuit Boards," Proc. 1997 IEEE International Symposium on EMC, pp.518-522, Jun. 1997.

[5] Clayton R. Paul, Introduction to Electromagnetic Compatibility. New York: Wiley, 1992.
[6] Todd H. Hubing, et al., "An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling," Proc. 1995 IEEE International Symposium on EMC, pp.518-522, Jul 1995.
[7] Shahrokh Daijavad, et al., "On the Effectiveness of Decoupling Capacitors in Reducing EM Radiation from PCBs," Proc. 1993 IEEE International Symposium on EMC, pp.518-522, Jan. 1993.
[8] Jun Fan, et al., "RF Isolation Using Power Islands in DC Power Bus Design," Proc. 1999 IEEE International Symposium on EMC, pp.838-843, May 1999.
[9] Todd H. Hubing, et al., "Power Bus Decoupling on Multi-layer Printed Circuit Boards," IEEE Trans. Electromagn. Compat., vol. 37, no.2,pp.155-166, May 1995.
[10] S. Van den Berghe, et al., "Study of the Ground Bounce Caused by Power Plane Resonances," IEEE Trans. Electromagn. Compat., vol. 40,no.2, pp.111-119, May 6 1998.
[11] Hao Shi, et al., "Modeling Multi-layered PCB Power-Bus Designs Using an MPIE Based Circuit Extraction Technique," Proc. 1998 IEEE International Symposium on EMC, pp.647-651, May 1998.
[12] Tatsuo Itoh, Numerical Techniques for Microwave and Millimeter-wave Passive Structures. New York: John Wiley & Sons, Inc., 1989 [13] Kuang-Ping Ma, et al., "Comparision of FDTD Algorithms for Sub-cellular Modeling of Slots in Shieding Enclosures," IEEE Trans. Electromagn. Compat., vol.39, no.2, pp.147-155, May 1997.
[14] C. David Turner, Larry D. Bacon, "Evaluation of a Thin-Slot Formulation for Finite-Difference Time-Domain Electromagnetics Codes, " IEEE Trans. Electromagn. Compat., vol. 30, pp.523-528, Nov. 1988.
[15] Douglas J. Riley, C. David Turner, "Hybrid Thin-Slot Algorithm for the Analysis of Narrow Apertures in Finite-Difference Time-Domain Calculations, " IEEE Trans. Antennas and Propagation, vol. 38, no. 12, Dec. 1990.
[16] Bing-Zhong Wang, "Enhanced Thin-Slot Formalism for the FDTD Analysis of Thin-Slot Penetration, " IEEE Microwave and Guided Wave Letters, vol. 5, no. 5, May 1995.
[17] Ammar B. Kouki, Raj Mittra, Chi Hou Chan, "Analysis of a Thin Slot Discontinuity in the Reference Plane of a Microstrip Structure, " IEEE Trans. Microwave Theory and Techniques, vol. 41, no. 8, Aug. 1996.
[18] Guang-Tsai Lei, Robert W. Techentin, Barry K. Gilbert, "High-Frequency Characterization of Power/Ground-Plane Structures, " IEEE Trans. Microwave Theory and Techniques, vol. 47, no.5, pp.562-569, May 1999.
[19] Karl S. Kunz, Raymond J. Luebbers, The Finite Different Time Domain Method for Electromagnetics, CRC Press, 1993.
[20] Roger F. Harrington, Time-Harmonic Electromagnetic Fields, McGraw-Hill International Editions, 1976.
[22] J. G. Yook, V. Chandramouli, L. P. B. Katehi, K. A. Sakallah, T. R. Arabi, and T.A. Schreyer,“ Computation of switching noise in printed circuit boards,” IEEE Trans. Comp., Packag., and Manufact., Mar. 1997.
[23] G. T. Lei, R. W. Techentin, and B. K. Gilbert,“ High-frequency characterization of power/ground-plane structures,” IEEE Trans. Microwave Theory Tech., vol. 47, pp.562-569, May. 1999.
[24] S. Van den Berghe, F. Olyslager, D. De Zutter, J. De Moerloose and W.Temmerman,“ Study of the ground bounce caused by power plane resonances,” IEEE Trans. Electromagn. Compat., vol. 40, No. 2, May 1998.
[25] W. Cui, X. Ye, B. Archambeault, D. White, M. Li, and J.L. Drewniak,EMI Resulting from Signal Via Transitions through the DC Power Bus,” in Proc. Of IEEE Int. Symp. on EMC, 2000, pp. 821-825.
[26] 多層印刷電路板電源平面共振 之修訂線方法分析 Multi-Layered PCB Pwer Plane Resonance Analysis Using Modified Method of Lines 賴明佑 June. 2000 [27] 多層高速數位電路板中接地彈跳雜訊對電源品質及其電磁輻射效應之模擬與量測 Effect of Ground Bounce Noise on the Power Integrity and EMI Performance in Multi-Layered High-Speed Digital PCB 黃竣南 June. 2002.