Incremental Floorplanning by Using Corner Block List Representation

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ABSTRACT

Floorplanning is a very important step of physical design in the backend of IC design. As VLSI/SOC systems become more complex, it is probably necessary to reperform floorplanning process for obtaining a better solution if the initial result is unsatisfied. However, it is extremely time consuming to repeatedly perform floorplanning process. For this reason, the idea of incremental floorplanning is adopted to shorten the time and achieve quick physical design closure. In the thesis, the Corner Block List non-slicing representation is used to record the relative positions among modules and obtain an initial floorplanning result. For the initial floorplanning solution, a series of incremental operations will be performed, such as inserting modules, deleting modules and modifying modules. To mostly preserve the original positions relationship among modules, just a few modules are selected for simulated annealing process in doing each operation. There are two strategies for selecting modules in the proposed incremental algorithm. Experimental results show that the proposed incremental floorplanning algorithm has good performance especially in dealing with instances with small changes.

Keywords : floorplanning ; incremental floorplanning ; Corner Block List

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