植基於corner block list表示法之增量式平面規劃之研究

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摘 要

積體電路後端實體設計(physical design)中，平面規劃(floorplanning)一直是一個相當重要的設計步驟。然而隨著VLSI/SOC系統的複雜化，有可能在平面規劃結束後，因佈局結果不良，需重新再進行平面規劃以求得一較佳佈局結果。但若一再地重複進行平面規劃，這是相當耗時的。因此我們利用增量式平面規劃(incremental floorplanning)的觀念，縮短重複進行平面規劃的時間。 在本論文中，我們以Corner Block List(CBL)不可切割表示法來記錄模組間相對位置關係並得到一原始平面規劃圖。針對原始平面圖執行一連串增量式運算，包含新增模組、刪除模組與修改模組三種運算。為了盡量維持初始平面圖中模組間相對位置關係，不重新進行完整的平面規劃，因此提出兩種挑選少數模組進行模擬退火的策略，以得到面積較小與繞線長度較短的平面規劃圖。 實驗結果顯示所提增量式平面規劃演算法確實具有不錯的效能，且在少數模組維度小幅修改時，能產生不錯的平面規劃結果。

關鍵詞 : 平面規劃 ; 增量式平面規劃 ; Corner Block List

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