Implementation of Burst-Error-Decoding Algorithm of Reed-Solomon Codes Based on Embedded System

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ABSTRACT

A Reed-Solomon codes was already verified to be a kind of powerful error control code. It has quite high detecting and correcting of the multiple errors. Correcting of burst errors and random errors simultaneously is its advantage, which has been implemented in many systems. Because an RS code structured in Galois field, when the number elements in Galois field increases, its decoding complexity grows. In this thesis, the implementation of a burst error decoding algorithm for Reed-Solomon codes is presented. Trap-decoding based, detecting and correcting of burst errors in this algorithm are implemented in a FPGA embedded system. In the implementation process, both C and VHDL programming languages and a soft ware called System Generator are employed to realize this decoding algorithm, which is then downloaded into a FPGA embedded system. In the verification process, burst errors are corrected in this embedded system and then corrected data sent back to a computer via RS-232 transmission line. From the results of synthesized circuits, the decoding speed and hardware resources of VHDL implementation are faster and less than those of System Generator, respectively. As a code length increases, more hardware resources are utilized, and the corresponding decoding speed is slow down.

Keywords : Reed-Solomon codes ; burst error correcting algorithm ; embedded system ; error control code

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