

應用軟/硬體協同設計於影像處理系統之開發

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摘要

閾值運算於影像處理之應用相當廣泛，由於影像中每一個物體各自擁有其灰階分佈，因此藉由閾值之使用便能一一將物體提取出來。但既有的演算法較為複雜，運算也相當費時，難以有效實現於硬體電路中。因此本文便基於硬體電路設計之觀點，提出HGEM (Histogram-based Gaussian Estimation Method)閾值演算法，並將Sobel邊緣偵測與HGEM演算法實現於Xilinx Virtex-4 (XC4VLX25) FPGA晶片中，其運算速度可達193.9 MHz，相當於每秒可處理1479張256 × 256之灰階影像，已達到即時影像處理系統之需求。但在許多不同的應用中，單一的影像閾值並無法有效進行多物體的擷取與分類，因此便需要仰賴多閾值選取的演算法。雖然Otsu演算法可擴展至多閾值之運算，但由於疊代次數過高之問題，會需要相當長的運算時間。因此本文基於Otsu演算法，提出全新架構之多閾值演算法，亦即為TSMO (Two-Stage Multithreshold Otsu method)演算法，其做法是將整個閾值之搜尋範圍，分為兩階段來進行，藉由降低疊代次數來提升演算法執行之效率。由實驗結果可知，當TSMO採用32個分區數時，與Otsu演算法之結果相互比較，其誤差平均小於1%，而於5個閾值運算之情況，其運算速度可提升至超越10萬倍之效能。

關鍵詞：邊緣偵測；Otsu；HGEM；TSMO；FPGA

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