SW-Log-MAP Turbo Code Decoder with Asymmetric Length Sliding Window

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ABSTRACT

In this thesis, we propose a novel structure of Turbo code decoders used in 3GPP systems. Based on the SW-Log-MAP technology, the initial values of the backward state metric are estimated by the forward state metric. In order to further increase the accuracy of the estimated initial values, different-length windows for the backward and forward metrics are adopted. The simulation results show that the correctness of initial values and asymmetric length sliding windows (SW) can improve the performance of the turbo code decoder. Although the length of the SW is decreased by 50%, the bit error rate doesn't increase. The decoding delay are lower 25% than that of conventional decoder structure. In addition, under the required BER of 3GPP, the number of iterations per frame is only three. This will increase the throughput of the turbo code decoder. In addition to the performance evaluation, the Turbo code decoder with the proposed hardware architecture is also implemented and verified by using Verilog HDL in this thesis. Comparing to the traditional Turbo code decoder hardware architecture, the size of M1 memory can be reduced about 29.2%. Furthermore, the required memory of the proposed SISO decoder is reduced about 46.6% than that total of the traditional SISO decoder. However, the required logic elements have increased by about 11.6%

Keywords : Turbo Code Decoder ; SW-Log-MAP ; Verilog HDL ; 3GPP

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