非對稱長度移動視窗渦輪碼解碼器之研究

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摘 要

在本論文中，我們提出新的實現符合3GPP規格的渦輪碼解碼器（Turbo Code Decoder）架構，採用以前向狀態路徑估測做為後向狀態路徑的初始值，並提出非對稱長度的移動視窗，以增加後向狀態路徑值的正確性來改善渦輪碼解碼器的性能。從模擬結果顯示初始值的使用及非對稱長度視窗的架構，可以有效的產生更可靠的後向狀態路徑初始值，雖然縮減基本架構解碼視窗長度50%，但仍然不會提升BER，反而降低解碼延遲時間25%。並且發現只需3次的遞迴（Iteration）就可將BER降至3GPP規格的範圍內，這將會大幅提升整個解碼器速度。　　在硬體方面，本論文以Verilog HDL來驗證硬體架構並實現非對稱長度移動視窗架構。除此之外，本論文也提出把分支路徑計算器（BMC）提前在記憶體M1儲存接收符元值時計算出，並將記憶體M1改儲存分支路徑值，可以減少記憶體M1約29.2%，對SISO解碼器可以減少整體使用的記憶體約46.6%，不過使用的邏輯元件數會增加約11.6%。整體而言，本論文提出的架構設計並不影響整個系統的複雜性，但可增快解碼速度，提供現今3GPP系統中的渦輪解碼器多一種高速且小面積的硬體設計選擇。

關鍵詞 : 渦輪碼解碼器 ; SW-Log-MAP ; Verilog HDL ; 第三代行動電話

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