FPGA based a realization of BCH step-by-step decoding

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ABSTRACT

In general, an algebraic decoder is with high hardware complexity or a conventional step-by-step decoder is with long decoding delay, and both of them are not efficient for a cyclic code in terms of decoding complexity. In order to overcome this difficulty, a modified step-by-step decoding is proposed in this thesis, which increases the decoding speed of conventional step-by-step decoding. Comparing to algebraic decoding, it reduces hardware complexity. Especially, as the error correcting capability is no more than 3, modified step-by-step decoding needs less decoding delay than algebraic decoding and conventional step-by-step decoding do. In this thesis, a design of remainder circuits, syndromes, the syndrome-matrix determinant is implemented to detect and correct errors. In verification of the designed implementation, the VHDL code of the proposed decoding algorithm for a BCH code are first downloaded to a FPGA board, and data are transmitted from a computer via an RS232 interface. After a solution is ready on the FPGA board, and then transmitted back to the computer and check whether it is correct. In the results, the modified step-by-step algorithm holds better decoding speed and little more hardware complexity in comparison with the conventional step-by-step algorithm and can improve the drawbacks of the algebraic algorithm for BCH codes.

Keywords : cyclic code, BCH code, error control coding.

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