以 FPGA 為基礎完成二位元 BCH code 步階式解碼電路之實現

周文政、胡大湘

E-mail: 9511440@mail.dyu.edu.tw

摘 要

習知利用代數解碼法及步階式解碼法所設計之解碼器，因分別具有硬體複雜度高及解碼耗時之缺點，故無法對循環碼進行高效率解碼，而為了改善習知缺失，本論文係提出一種改良型步階式解碼演算法，其主要是針對BCH碼的改錯電路及其演算法進行改良設計；在功效上改良式步階解碼法在錯誤量較少 的情形下，其解碼過程中所耗費的時間，較代數解碼法與傳統步階式解碼法為少。 本論文係改良傳統步階式解碼演算法，利用組合電路設計並進行餘式、徵狀、徵狀矩陣及行列式值之計算。而驗證上，係將設計完成之BCH解碼器的VHDL程式碼下載至FPGA實驗板，並自電腦端以RS232介面傳送訊息資料至FPGA端進行計算，待FPGA端計算完成後，回傳計算結果至電腦端，再以超級終端機檢視其更正結果。 本論文所得之結果，在解碼速度上，比傳統步階式解碼法快，且硬體複雜度近似傳統步階式解碼法，本論文所改良的步階式解碼演算法係可有效改善代數解碼法之硬體複雜度過高及傳統步階式解碼法解碼耗費之問題。

關鍵詞 : 循環碼，BCH碼，錯誤更正碼。

目錄

參考文獻

[1] S. Lin and D. J. Costello, Jr, Error Control Codin, Prentice Hall, 2004.

[2] J. Massey, “ Step-by-step decoding of the Bose-Chaudhuri- Hocquenghem codes, ” IEEE Transactions on Information Theory, Vol. 11, No. 4, pp. 580-585, Oct 1965.

[3] Z. Szwaja “ On step-by-step decoding of the BCH binary codes, ” IEEE Transactions on Information Theory, Vol.13, No.2, pp.350-351, Apr. 1967.

[4] S.W. Wei, and C.-H.Wei, “ A high-speed real-time binary BCH decoder, ” IEEE Transactions on Circuits and Systems for Video Technology, Vol. 3, No. 2 , pp.138-147,April 1993.

[5] C. L. Chr , Szu-Lin. Su and Shao-Wei. Wu, “ New step-by-step decoding for binary BCH codes, ” The Ninth International Conference on Communications Systems, 2004. ICCS 2004. pp. 456-460, Sept. 2004.

[6] S. W. Wei, and C.H. U ’ ei , “ High speed hardware decoder for double-error correcting binary BCH codes ”. IEE Proceedings, vol. 136. Pt.

I, no. 3, June 1989.
[7] S. A. Abbasi, “ FPGA based realization of a reduced complexity high speed decoder for error correction, ” ICECS 2003. Proceedings of the 2003 10th IEEE International Conference on Electronics, Circuits and Systems, 2003,Vol. 3, pp.1002-1005, Dec. 2003.
[8] E. -H. Lu and T. Chang, ” New decoder for double-error-correcting binary BCH codes, ” IEE Proceedings Communications,Vol. 143, Issue 3, pp.129-132, June 1996.
[9] Kraft. C, ” Closed solution of Berlekamp's algorithm for fast decoding of BCH codes, ” IEEE Transactions on Communications, Vol. 39, Issue 12, pp.1721-1725, Dec. 1991.
[10] G. -L. Feng and K. K. Tzeng, ” A generalized Euclidean algorithm for multisequence shift-register synthesis, ” IEEE Transactions on Information Theory,Vol. 35, Issue 3, pp.584-594, May 1989.
[11] M. -H. Cheng, ” Generalised Berlekamp-Massey algorithm, ” IEE Proceedings Communications,Vol. 149, Issue 4, pp.207-210,Aug. 2002.
[12] M. Srinivasan and D. V. Sarwate, ” Malfunction in the Peterson-Gorenstein-Zierler decoder, ” IEEE Transactions on Information Theory, Vol. 40, Issue 5, pp.1649-1653, Sept. 1994.
[13] W.M.EI-Medany , C.G.Warrison , P. G. Farrell.and C. J. Mardf, ” VHDL implmentation of a BCH minimum weight decoder for double error, ” Radio Science Conference, 2001. NRSC 2001. Proceedings of the Eighteenth National,Vol. 2, pp.27-29, March 2001.
[14] Lijun Zhang , Victor O. K. Li and Zhigang Cao ” Short BCH codes for wireless multimedia data, ” Wireless Communications and Networking Conference, 2002. WCNC2002. 2002 IEEE,Vol. 1, pp.220-222,March 2002.
[15] W. W. Peterson, ” Encoding and error-correction procedures for the Bose-Chaudhuri codes, ” IEEE Transactions on Information Theory,Vol. 6, Issue 4, pp.459-470,Sep 1960.
[16] R. T. Chien, ” Cyclic decoding procedures for Bose- Chaudhuri-Hocquenghem codes, ” IEEE Transactions on Information Theory,Vol. 10, Issue 4, pp.357-363,Oct 1964.
[17] D. J. Jr. Costello , J. Hagenauer , H. Imai and S. B. Wicker, “ Applications of error-control coding, ” IEEE Transactions on Information Theory, Vol. 44 , No. 6, pp.2531-2560, Oct. 1998.
[18] G. JR. Forney, “ Generalized Minimum Distance Decoding, ” IEEE Trans. Inform. Theory, Vol .IT-12, No 2. pp.125-131, Sept. 1966.
[19] H. Helgert , R. Stinaff, “ Shortened BCH codes, ” IEEE Transactions on Information Theory, Vol. 19, No.6, pp. 818-820, Nov 1973.