ESD Implantationsin in Sub-Quarter-Micron Bulk CMOS Technology

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ABSTRACT

In enduring the nano CMOS integrated circuit, the static discharges (ESD) the protective capacities are reduced by a wide margin as the size of the component is reduced , traditional ESD already to protect circuit design and method can't bear using, endure nano system ESD protect component select and ESD protect circuit it designs to be must in order to improve. We have initial NMOS component which lead open characteristic already-on (native) to one, study its ESD component characteristic, and propose its innovative application in enduring the rice CMOS integrated circuit. This kind of already-on (native) NMOS component has characteristic lower or of shouldering the critical voltage (threshold voltage more). When IC is shelled by ESD, this kind of already-on (native) component will lead the open characteristic initially , that is to say, when IC floats and connects , this kind of already-on (native) component will be leading the open state and coming down to wait for the bombardment of ESD. So this kind of already-on (native) component has leading the open speed and the lowest voltage of touching off fast most in theory . Like this , could protect in endure metric system ultrathin Gate Oxide layer in the Cheng efficient (thickness is smaller than 15A). IC is under the general normal running , in order to make this kind of already-on (native) component shut off and avoid unnecessary leaking the electric current, the bar of this component needs to add the passway where the bias voltage of a loss shut off the component .

Keywords : already-on (native) component, NMOS, ESD

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