Reducing Crosstalk by Buffer Insertion with Post-Layout Area Slack

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ABSTRACT

With the rapidly advancing semiconductor fabrication technologies, the feature sizes of device and interconnection of an integrated circuit are shrunk distinctly. Thus, the coupling and fringe capacitances of wires becomes more significant on the effect of performance of modern circuits. In addition, the induced crosstalk between two closed parallel interconnections may cause serious degradation of timing delay of the victim net of the interconnections in a circuit. Therefore, how to reduce the crosstalk is an important issue in the design of modern circuits. Buffer insertion is one of the effective ways to alleviate crosstalk of a circuit. However, if the placement information is not taken into consideration while applying the buffer insertion process, the area overhead will obviously increase in the resulted circuit. It will not only raise the cost of a circuit, but also increase the dissipated energy and decrease the fabrication yield of the circuit. In this paper, we propose an algorithm first extracting the white spaces from the layout after the placement and routing process of a standard-cell design. These area slacks are used to reduce the crosstalk of the circuit with performing buffer insertion. Since the buffers are placed on the extracted white spaces, there is no area overhead in ours method. In order to gain most reduction of crosstalk by utilizing the area slacks, the white spaces are globally assigned to the victim nets. After the assignment of white space for inserting a buffer to a victim net, the original routing path of the victim net is split into two segments. Then, a maze-router is applied to locally modify the routing path to connect the segment from the source of the net to the input pin of the buffer and from the output pin of the buffer to the segment to the destination of the net. Experiments are performed on the circuits from the ISCAS89 benchmark suite with TSMC 0.18um standard-cell library. First, the commercial tool SOC Encounter is used to perform the placement and routing process and analyze the crosstalk of the circuits. After applying our crosstalk-reduction algorithm, the resulted circuits can successfully pass the DRC and LVS examination. A reduction of crosstalk about 75%, on the average, is achieved by our algorithm.

Keywords : area slack, crosstalk, buffer insertion, maze routing, VLSI/CAD.

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