

佈局後利用空間資訊以降低串音問題之探討

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摘要

在先進製程技術下，積體電路內部連接線的耦合(Coupling)與邊緣(Fringe)寄生電容大幅增加，引發明顯的訊號干擾(crosstalk)現象，導致訊號完整性(Signal Integrity)的嚴重問題，訊號干擾不僅會影響電路的效能，更嚴重者將造成電路功能不正確，因此，如何降低積體電路的訊號干擾，是目前一個很重要的研究議題。安插緩衝器(Buffer Insertion)是目前常用來降低訊號干擾的有效方案之一，但是安插緩衝器若不考慮電路佈局因素，則電路面積的增加量將相當明顯，這不僅增加電路的成本，且將造成電路功率消耗(power dissipation)增加與良率(yield)降低的不良現象。本篇論文探討在執行完電路元件擺置與繞線(Placement & Routing, R&R)後，進一步由佈局規劃中抽取未被使用的可用空間資訊，作為安插緩衝器之用，以降低電路同金屬層的訊號干擾。根據前述的可用空間，我們設計一套演算法，針對電路中訊號干擾較嚴重的連接線，整體分配使用這些寶貴的可用空間來安插緩衝器，使得訊號干擾現象可以得到最佳的改善。連接線的緩衝器位置安排完成後，再以Maze-Routing演算法來修改繞線的路徑。在實驗部分，以ISCAS 89 測試電路組來做分析，搭配TSMC 0.18um 製程標準元件庫，並且利用SOC Encounter 這套佈局軟體，作為訊號干擾分析的工具。電路經過本文所設計的安插緩衝器程序後，除都可以順利通過DRC與LVS的驗證之外，獲得訊號干擾降低比率約75%以上。

關鍵詞：空間資訊，緩衝器安插，訊號干擾，佈局

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