

Fabrication and Characterization of Fe-doped InP/InGaAs HEMTs

陳永聖、蕭宏彬

E-mail: 9511200@mail.dyu.edu.tw

ABSTRACT

The performance of the InP-based FETs is limited due to the quality of the Schottky contact that results in high gate leakage current. In order to enhance the quality of Schottky contact, a wide bandgap material InAlAs was adopted to increase Schottky barrier height and reduce the gate leakage current. However, the InAlAs always suffers the oxidation of aluminum. The process to form the gate metal on the InAlAs surface will become very tough for obtaining a good quality of Schottky contact. As the Fe-doped InP material shows very high resistivity, in this study we will deposit the gate metal on the Fe-doped InP to form a Schottky contact. We expect the gate leakage current should be reduced and the performance of InP-based FETs could be enhanced. Au was selected to be Schottky metal on Fe-doped InP, and Schottky barrier height is as high as 0.75eV. The saturation drain current for FETs with gate length of 5 was about 110 mA/mm at $V_{DS}=2.5$. The pinch-off voltage was around -1.75 V. A maximum intrinsic transconductance of 60 mS/mm was measured at $V_{GS}=+0.1$ V and $V_{DS}=2.5$ V. The breakdown voltage between gate to drain was larger than -4.5V.

Keywords : InP/InGaAs FETs ; Schottky contact

Table of Contents

封面內頁 簽名頁 授權書	iii	中文摘要	iii
.	iv	英文摘要	vi
.	vii	誌謝	vi
.	viii	目錄	viii
.	x	圖目錄	viii
.	x	第一章 緒論	1
1-1前言	1	1-2研究動機	2
1-2-1元件材料選擇	3	1-3-1磷化銦材料的優點	3
1-2-2磷化銦材料的優點	3	1-3-2砷化銦鎵材料的優點	3
1-2-3金屬-半導體歐姆接觸	3	1-4 HEMT歷史	4
1-2-4二維電子氣的電子原理	5	第二章 理論與原理	4
1-2-5二維電子氣的電子原理	8	2-1蕭特基能障二極體(Schottky Barrier Diode)	6
2-2蕭特基能障能障高的量測方法	8	2-2蕭特基能障能障高的量測方法	6
2-3金屬-半導體歐姆接觸	11	2-3金屬-半導體歐姆接觸	9
2-4高速電子移動電晶體的操作原理	11	2-4高速電子移動電晶體的操作原理	9
2-5二維電子氣的電子原理	12	第三章 元件製程方法	12
3-1磊晶結構設計	13	3-1-1表面覆蓋層設計	13
3-1-1表面覆蓋層設計	13	3-1-2蕭特基閘極接觸層設計	13
3-1-2蕭特基閘極接觸層設計	13	3-1-3主動通道層設計	14
3-1-3主動通道層設計	14	3-1-4緩衝層設計	14
3-1-4緩衝層設計	14	3-2蕭特基二極體製作	15
3-2蕭特基二極體製作	15	3-2-1元件製作程序	15
3-2-1元件製作程序	15	3-2-2金屬蒸鍍與Lift-off	16
3-2-2金屬蒸鍍與Lift-off	15	3-3 PHEMT 高電子遷移率電晶體元件製	17
3-3 PHEMT 高電子遷移率電晶體元件製	17	3-3-1高臺蝕刻 (Mesa Etching)	17
3-3-1高臺蝕刻 (Mesa Etching)	17	3-3-2汲極與源極歐姆接觸之製作	19
3-3-2汲極與源極歐姆接觸之製作	17	3-3-3閘極蕭特基接觸之製作	20
3-3-3閘極蕭特基接觸之製作	20	第四章 元件直流特性量測、分析與討論	22
第四章 元件直流特性量測、分析與討論	22	4-1蕭特基二極體電流-電壓特性曲線之量測	22
4-1蕭特基二極體電流-電壓特性曲線之量測	22	4-2電晶體電流-電壓特性曲線之量測	23
4-2電晶體電流-電壓特性曲線之量測	22	4-3互導值之量測	23
4-3互導值之量測	24	4-4 閘極-源極電流-電壓(IGS-VGS)之量測	25
4-4 閘極-源極電流-電壓(IGS-VGS)之量測	24	第五章 結論	25
第五章 結論	26	參考文獻	44
參考文獻	26		

REFERENCES

- [1] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, " A new Field-Effect Transistor with Selectively Doped GaAs/n-AlxGa1-xAs Heterojunctions," Jap. J. Appl. Phys, vol.19, no. 5, pp.225-227, 1980.
- [2] Nguyen, L.D.; Brown, A.S.; Thompson, M.A.; Jelloian, L.M. " 50-nm self-aligned-gate pseudomorphic AlInAs/GaInAs high electron mobility transistors," IEEE Transaction on Electron Devices, vol.39, no.9, pp.2007 – 2014,1992.
- [3] C.K.Peng, M.I.Akum, A.A.Vetterson, H.Morkoc, and K.R.Gleason, " Microwave performance of InAlAs/InGaAs/InP MODFET, " IEEE Electron Device Letters, vol.8, no.1, pp.24, 1987.
- [4] Mishra, U.K. Brown, A.S. Jelloian, L.M.; Hackett, L.H. Delaney, .J; " High-performance Submicrometer AlInAs/GaInAs HEMTs, " Electron Device Letters, IEEE, vol.9, no.1, pp. 41 – 43,1988.

- [5] K Armaned, D. V Bui, J Cheverier, and N. T. Lihn, " High-power microwave amplification with InP MISFET, " in Proc. IEEE/Cornell Conf. High Speed Semiconductor Devices and Circuits (Ithaca, NY). New York: IEEE Transaction on Electron Devices, pp.218-225,1984.
- [6] M. Smith, " Status of InP HEMT technology for microwave receiver applications, " IEEE Transaction on Electron Devices, Microwave Theory Tech.vol.44 no.8, pp. 2328-2333, 1996.
- [7] K Armaned, D. V Bui, J Cheverier, and N. T. Lihn, " High-power microwave amplification with InP MISFET, " in Proc. IEEE/Cornell Conf. High Speed Semiconductor Devices and Circuits (Ithaca, NY). New York: IEEE Electron Device Letters, pp.218-225, 1984.
- [8] L. Messick, D. A. Collins, R. Nguyen, A. R. Clawson, and G. E. McWilliams, " High-power high-efficiency stable indium phosphide MISFETs, " in IDEN Tech. Dig, pp. 767-770, 1986 [9] P. Saunier, R. Nguyen, L. J. Messick, and M. A. Khatibzadeh, " An InP MISFET with a power density of 1.8W/mm at 30 GHz, " IEEE Electron Device Letters, vol. 11, no. 1, pp. 48-49, 1990.
- [10] Klaus Schimpf, Michael Sommer, Manfred Horstmann, Martin Hollfelder, " 0.1- μ m T-gate Al-free InP/InGaAs/InP pHEMTs for W-bandapplications using a nitrogen carrier for LP-MOCVD growth, " IEEE Electron Device Letters, nol. 18, no. 4, pp.144-146, 1997.
- [11]W. Schottky, " Halbleiterteorie der Sperrschicht, " Naturwissenschaften, vol.26, p.843, 1938.
- [12] S. M. Sze, " Semiconductor Devices:Physics and Technology, " John Wiley & Sons, INC, 1985.
- [13] H.Craig Casey, JR " Devices For Integrated Circuits, " John Wily & Sons, INC, 1999.
- [14] Dieter K. Schroder, " Semiconductor Material and Device Characterization, " John Wiley & Sons, INC., 1997.
- [15] H. Craig Casey, JR., " DEVICES FOR INTEGRATED CIRCUITS Silicon AND - Compound Semiconductors, " John Wiley & Sons, INC, 1999.
- [16]辛裕明, " 磷化銦基體金屬-半導體場效電晶體之製造及其性, " 交通大學碩士論文, 1981.
- [17] Zs.J.Horvath, E.Ayyildiz, V.Rakovics " Schottky contacts to InP, " Wiley InterScience,vol. 2,no. 4,pp.1423-1427,2005.
- [18] A.A.Iliadis, " Schottky barrier height enhancement in n-InP, " in Gallium Arsenide and related compounds, Conf . Series, vol. 92, pp.413 ,1988.
- [19] Iliadis, A.A.; Lee, W.; Aina, O.A. " N-Channel Depletion-Mode InP FET with Enhanced Barrier Height Gates, " IEEE Electron Device Letters ,vol.10 , no.8, pp.370-372 ,1989.
- [20] 李世鴻, " 半導體物理及元件第三版 " ,台商圖書有限公司,2003.