Structural Model Design of a Synthesizable MIPS-like Microprocessor with Nonvolatile Memory Interfaces

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ABSTRACT

This study develops a 32-bit RISC processor core embedded with MIPS-like architecture by using Verilog HDL and algorithmic state machine (ASM). The designed processor core is carried out through the behavioral, mixed and structural stage by simulation of SynaptiCAD. Besides, the developed processor core is implemented into the FPGA chip for rapid verification with an application circuit to stepper motor control. Simulation and measurement results reveal that less number of gates is required during the synthesis work and overall design is correct. The designed machine code is also implemented in external nonvolatile memory to save gate utilization of FPGA chip.

Keywords : MIPS、ASM、Verilog、FPGA、Nonvolatile Memory

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