VLSI Layout of a Back-Propagation Neuro-Microprocessor

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ABSTRACT

This study develops a 32-bit RISC processor core embedded with first-order back-propagation neural network and MIPS-like architecture by using Verilog HDL and algorithmic state machine (ASM). The designed processor core is carried out through the behavioral stage by simulation of SynaptiCAD and synthesis of Xilinx FPGA development software. The VLSI layout of a neuro-microprocessor core is implemented under TSMC 0.18 um process technology at final.

Keywords : MIPS、ASM、Verilog、Back-propagation Neural Network

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REFERENCES

[1] www.doe.carleton.ca/~pavan/courses/resources-elec3500/verilog1 _notes. pdf [2] Werbos, P. J., Beyond regression: New tools for prediction and analysis in the behavioral sciences. Ph.D. Thesis, Harvard University, 1974.

[3] Werbos, P. J., Advanced forecasting methods for global crisis warning and models of intelligence. Gen. Syst. 1977, 22, 25-38.

[4] Werbos, P. J., Generalization of back-propagation with application to a recurrent gas market model. Neural Networks 1988, I, 339-356.

[5] Rumelhart, D. E., Hinton, G. E. & Williams, R. J., in Parallel Distributed Processing: Explorations in the Microstructure of Cognition. Vol. 1: Foundations (eds. Rumelhart, D. E. & McClelland, J. L.) 318.362 (MIT, Cambridge, 1986) [6] Mark Gordon Arnold, “ Verilog Digital Computer Design: Algorithms into Hardware ”, Prentice Hall PTR, 1999, Chap. 8, pp. 277-353.

[7] Mark Holland, “ Harnessing FPGAs for Computer Architecture Education ”, University of Washington, 2002.

[8] David A. Patterson & John L. Hennessy, “ Computer Organization & Design: The Hardware/Software Interface ”, Morgan Kaufmann, December 1997. -54- [9] MIPS Technologies Inc., “ Introduction to the MIPS32 Architecture ”, MIPS Technologies, Inc.

[10] Kab Joo Lee; “ Fault sensitivity analysis of a 32-bit RISC microprocessor ”, VLSI and CAD, ICVC '99. 6th International Conference, 1999, pp. 529-532 [11] David A. Patterson & John L. Hennessy, “ Computer Organization & Design: The Hardware/Software Interface ”, 2nd Edition Published by Morgan Kaufmann, Dec. 1997, Chap. 3, pp. 3-1 to 3-113.

[12] “ Introduction to the MIPS32 Architecture ”, MIPS Technologies Inc., 2001.

[13] “ MIPS32TM Architecture For Programmers Volume I: Introduction to the MIPS32TM Architecture ”, MIPS Technologies Inc., March 2001.

[14] William Stallings, “ Reduced Instruction Set Computer Architecture ”, Proceedings of the IEEE, Vol. 76, No. 1, Jan. 1988, pp. 38-55.

[15] Mark Gordon Arnold, “ Verilog Digital Computer Design: Algorithms into Hardware ”, Prentice Hall PTR, 1999, Chap. 2, pp. 7-63.

[16]Ilya Levin, Vladimir Sinelnikov and Mark Karpovsky, “ Synthesis of ASM-based Self Checking Controllers ”, IEEE, 2001, pp. 87-93.

[17] 王進德、蕭大全 (民92)，類神經網路與模糊控制理論入門，全華科技圖書股份有限公司， 台北市。 -55- [18] 林昇甫、洪成安 (民82)，神經網路入門與圖辨識，全華科技圖書股份有限公司，台北市。

[19] A. K. Rigler, J. M. Irvine and T. P. Vogl, "Rescaling of variables in backpropagation learning," Neural Networks, vol. 4, no. 2, pp. 225 --229, 1991.

[20] S. Grossberg, E. Mingolla, and D. Todovoric, "A neural network architecture for preattentive vision," IEEE Trans. Biomed. Eng., 36:65--83,

1989 [21] Barnard, E., "Optimization for training neural nets," IEEE Trans. Neural Network, vol. 3, pp. 232 --240, Mar. 1992 [22] Hagan, M.T. and Menhaj, M.B., "Training feedforward networks with the Marquardt algorithm," IEEE Trans. Neural Network, vol. 5, pp. 989 --993, Nov. 1994 [23] Pei-Yih Ting and Iltis, R.A., "Diffusion network architectures for implementation of Gibbs samplers with applications to assignment problems," IEEE Trans. Neural Network, vol. 5, pp. 622 --638, July 1994 [24] 曾榮鴻, 莊季高 (民91)，碩士論文，類神經網路應用於數字識別之分析與比較，國立海洋大學。
[25] 曾憲輝 (民89)，碩士論文，以雙向聯想記憶網路為設計基礎 之智慧晶片，逢甲大學。
[26] 葉怡成，應用類神經網路(民88)，儒林圖書有限公司，台北市。
[27] 林柏宏(民91)，碩士論文，類神經網路應用於雙相氣泡流相傳遞特性之即時決定，大葉大學。