倒傳遞類神經微處理器之超大型積體電路佈局

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摘 要

本研究利用Verilog硬體描述語言(Hardware Description Language, HDL)和演算法狀態機制 (Algorithmic State Machine, ASM)發展一個內嵌一階倒傳遞類神經網路(First-Order Backpropagation Neural Network)似MIPS架構之32位元精簡指令集處理器核心，進行行為模式設計， 並配合SynaptiCAD模擬與Xilinx FPGA晶片軟體合成，最後並完成台積電0.18微米製程的超大型積體 電路佈局設計。

關鍵詞 : MIPS、ASM、Verilog、Back-propagation Neural Network

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