A Pipeline Backpropagation Neuro-Microprocessor

謝元章、陳木松、陳慶順

E-mail: 9510652@mail.dyu.edu.tw

ABSTRACT

The study develops a pipelined 32-bit microprocessor embedded with first-order back-propagation neural network and MIPS-like architecture by using Algorithmic State Machine(ASM) and Verilog HDL. The designed neural network is verified by using Matlab. The Matlab source code is derived into MIPS-like assembly and machine code to be embedded in processor core. With the comparison of the simulation result of SynaptiCAD and Matlab, the verified processor core is further synthesized by using Xilinx FPGA development software. The VLSI layout of developed neuro-microprocessor is implemented under TSMC 0.18 um process technology at final.

Keywords : ASM, Pipeline, Back-propagation Neural Network, MIPS, Verilog.

Table of Contents

REFERENCES

[1] Rumelart, D.E., Hinton, G.E. and Williams, R.J.“ Learning internalrepresentation by error propagation ”, in Parallel Distributed Processing, Vol.1,318-326,1986.

[2] Sung Su Kim, Seul Jung,“ Hardware implementation of a real time neural network controller with a DSP and an FPGA ”,Robotics and Automation, Proceedings. IEEE International Conference on, Volume 5 Page:4639 – 4644, 2004.

[3] Arnold, M.G., T.A. Bailey J.R. Cowles J.J. GupalF.N,“ Behavior to Structure: Using Verilog andIn－Circuit Emulation to Teach How An AlgorithmBecomes Hardware ”, Engineer, IEEE, Verilog HDL Conference, P19-28. 1995.

[4] Arnold, M.G.“ Verilog Digital ComputerDesign Algorithms into Hardware ”, 2001.

[5] Mark Holland,“ Harnessin FPGAs for Computer Architecture Education, ”A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science In Electrical Engineering, University of Washington, 2002.

[6] 蔡安朝, 陳慶順, 潘天賜,“ 實現一個運用似MIPS架構之步進馬 達控制系統晶片 ”，中華民國自動控制研討會，大葉大學，2004。

[7] 劉俊佑, 陳慶順, 洪榮聰,“ 發展運用似MIPS架構之微控制 器 ”，中華民國自動控制研討會，大葉大學，2004。

[8] 林右文, 陳慶順, 呂嘉弘,“ 以FPGA實現交通號誌控制器 ”，中 華民國自動控制研討會,大葉大學，2004。

[9] Golden, M., Mudge, T.,“ Comparison of two common pipeline structures ” Computers and Digital Techniques, IEE Proceedings , Volume: 143 , Issue: 3 ,Pages:161 - 167,1996.

[10] 王進德、蕭大全,“ 類神經網路與模糊控制理論入門 ”，全華科 技圖書股份有限公司，2003。

[11] Kab Joo Lee,“ Fault sensitivity analysis of a 32-bit RISC microprocessor ” VLSI and CAD, ICVC '99. 6th International Conference, pp. 529 - 532, 1999.

[12] Mark Gordon Arnold,“ Verilog Digital Computer Design: Algorithms into Hardware ”, Prentice Hall PTR, pp. 7-63, 1999.

[13] Ilya Levin, and Mark Karpovsky,“ Synthesis of ASM-based Self Checking Controllers ”, IEEE, pp. 87-93, 2001.

[14] CIC reference, Cell-Based IC Design Concepts, 2003.

[15] 曾志光 鄭光廷,“ 計算機組織與設計 軟硬體介面 ”，碁.，第 三、五章，3-2~5-43，2000。

[16] Liu Zhenyu , Qi Jiayue “ Implementation of precise exception in a 5-stage pipeline embedded processor ” ASIC, Proceedings. 5th International Conference on Volume: 1 , 21-24,Pages:447 - 451 Vol.1, 2003.
[17] Rigler, A. K., Irvine, J. M. and T. P. Vogl, “ Rescaling of variables in backpropagation learning, ” Neural Networks, vol. 4, pp. 225 -229, 1991.
[18] Barnard, E., “ Optimization for training neural nets, ” IEEE Trans. Neural Network, vol. 3, pp. 232 -240, Mar , 1992.
[19] Hagan, M.T. and Menhaj, M.B. “ Training feedforward networks with the Marquardt algorithm, ” IEEE Trans. Neural Network, vol. 5, pp. 989 -993, Nov., 1994.
[20] “ Open Floating Point Unit ” http://www.opencores.org.
[21] 張耀祖 白煌朗 方偉平, “ 數值分析 ”, 松崗電腦圖書資料股份 有限公司, 第三章, 1991。
[22]H.T. Bui, B. Khalaf and S. Tahar: “ Table-Driven Floating-Point Exponential Function ” Technical Report, Concordia University,Department of Electrical and Computer Engineering, October 1998.
[23]Ping Tak Peter Tang. “ Table-Driven Implementation of the Exponential Function in IEEE Floating-Point Arithmetic. ” ACM Transactions on Mathematical Software. vol.no.2.1989.
[24] 葉怡成, “ 應用類神經網路 ” 儒林圖書有限公司, 台北, 1989。
[25] 林柏宏, 碩士論文, “ 類神經網路應用於雙相氣泡流相傳遞特 性之即時決定 ” 大葉大學, 2002。
[26] Asai, T.; Yokotsuka, H.; Fukai, T. “ A MOS circuit for a nonmonotonic neural network with excellent retrieval capabilities ” Volume 7, Issue 1, Page:182 -189,1996.
[27] 曾榮鴻 莊季高, 碩士論文, “ 類神經網路應用於數字識別之 分析與比較 ”, 國立海洋大學, 1992。
[28] Christopher M. Bishop “ Exact Calculation of the Hessian Matrixfor the Multi-layer Perceptron ” Published in Neural Computation 4 No. 4494 -501 , 1992.
[29] Guimaraes, F.G.; Ramirez, J.A.;Magnetics, “ A Pruning Method for Neural Networks and ItsApplication for Optimization in Electromagnetics ” IEEE Transactions onVolume 40, Part Page:1160-1163 Digital Object Identifier, 2004.