A Cache Design of Network Processor

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ABSTRACT

Network processors are mostly designed in SOC architecture. To hasten the design schedule and retain flexibility, network protocols are often implemented in software. Considering this, design optimization is no longer an isolated issue but collaboration between hardware and software. In general, modern micro-architecture design relies on dynamic instruction traces to provide necessary information for design optimization. One of the drawbacks of dynamic instruction traces is it generates massive data that make it difficult to process and store. This thesis proposes a novel profiling scheme and a dynamic instruction profiling algorithm that called Melting. Using the proposed profile scheme, the profiling is done in hierarchy that reduces the data generated. The proposed profiling scheme will also extract the most frequent and longest instruction sequence. The extracted sequence is used in optimizing memory hierarchy. The SimpleScalar ARM 4.0 simulator with Dijkstra benchmark form MiBench is setup to verify our profiling scheme.

Keywords : Network processors ; trace ; profiling ; SimpleScalar ; Dijkstra

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