網路處理器快取記憶體設計

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摘 要

網路處理器使用SOC的架構，為減少開發時程，及保留更動的彈性，屬於協定層演算法的部份多採軟體方式實現，因此最佳化設計方法不再是軟體或硬體獨立事件，而需依賴軟硬體協同設計的手段。一般處理器微架構設計多依賴動態指令層追蹤分析供最佳化的參考。動態指令層追蹤分析常有追蹤耗時、資料龐大處理困難的問題。 本文提出一個新的方法，稱為動態指令側描及一個命名為Melting的演算法，可使用階段性的步驟來解決上述問題，並找到出現次數最頻繁的最長指令序列，可供網路處理器微架構最佳化設計參考。最後使用SimpleScalar ARM 4.0模擬器搭配MiBench的Dijkstra效能測試程式來驗證我們所提出來的方法。

關鍵詞 : 網路處理器 ; 模擬器 ; 最佳化設計 ; 動態指令層追蹤 ; 效能分析

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