

High-Speed Parallel Cyclic Redundancy Check Circuit

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ABSTRACT

Error Control Coding is widely used in data communications and storage devices as a powerful method for dealing with data errors. It also applies to many other fields such as the testing of integrated circuits and the detection of logical faults. In this thesis, we develop the advanced parallel Burst Error Correcting Code circuits. We use combinational circuit to compute syndrome and error patterns, and using FPGA board to implement our Fire Code Decoder.

Keywords : Error Control Coding, CRC, Burst Error, LFSR, FPGA

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