高速平行處理架構之循環冗餘檢查碼電路

張力元、胡大湘 ; 洪進華

E-mail: 9501987@mail.dyu.edu.tw

摘 要

在目前科技日新月異之下，資料的傳輸也愈來愈快，傳輸上的錯誤也會一直不斷的發生。錯誤控制編碼(Error control Coding)，在對於處理資料傳輸上的錯誤是一種非常有用的方法，並且被廣泛的使用在資料通訊傳輸上及儲存系統上。錯誤控制編碼可以確保我們在接收資料時的正確性，也可以用在測試積體電路以及邏輯電路的錯誤。 本論文是針對Burst Error 、 Serial CRC改錯電路作Parallel之運算，改善其架構，輸入資料以平行輸入之方式，利用組合電路，計算其Syndrome，以及Error pattern，改錯部分也是以平行處理的方式計算。將設計好之Fire Code Decoder電路download至FPGA實驗板，利用電腦端RS232傳輸，將其資料傳送至FPGA，等待FPGA端計算完成之後傳送至電腦端看其更正結果。

關鍵詞 : 改錯碼、循環檢測碼、Parallel CRC、LFSR、VLSI、digital logic、 Error Control Coding

目錄

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