發展運用似MIPS架構之微控制器

劉俊佑、陳慶順

E-mail: 9419998@mail.dyu.edu.tw

摘 要

本研究利用Verilog硬體描述語言(Hardware Description Language, HDL)發展似MIPS 架構之32位元 精簡指令集微控制器RISC，研發過程以Behavioral，Mixed 及Structural 三階段型式進行。 Behavioral 設計階段於現場可程式化閘陣列(Field Programmable Gate Array, FPGA) 上實現 並以應用電路驗證，且Behavioral，Mixed 及Structural 不同設計階段結果也運用模擬方式加以 進一步驗證。

關鍵詞 : 精簡指令集微控制器、硬體描述語言

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