The Design and Implementation of Built-In Scan Delay Measurement Cell

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ABSTRACT

The accurate delay measurement is a major issue to test advanced SoC chips. The low/noisy supply voltage induces CUT delay, and makes the SCAN testing technique hard to capture the correct output delay responses. In this thesis, we propose a built-in delay testing (BIDT) methodology, which combine the delay detection circuit (BIDT), Built-in test (BIST) and scan chain methodologies into together. The BIDT circuitry does not only provide the feasible internal delay test/measurement mechanisms, but also provide the adaptive clock timing to assist the scan chain capture the correct output responses for preventing delay test errors. Our methodology will be very useful for measuring the correct circuit performance in complex/high-speed SoC dies. The contribution of our works is proposing a feasible delay measurement method to reduce the yield lose from performance test killing errors. This work also tries to propose a practical delay fault determine technique under low/noisy voltage testing environment. In the experiments, we first calculate the circuit delay by using a new voltage-aware static timing analysis (STA) tool, which could measure the CUT delay under varying supply voltage. The experiments then show the correct path delay could be observed form the scan chain under jointing the factors of voltage drop come from IR-drop. The real BIDT chip is implemented by using TSMC 0.18um and validated functional correct finally.

Keywords : BIST , Delay testing , Scan chain

Table of Contents

第一章 緒論 1.1 研究動機. . . . . 1 1.2 研究目標. . . . . 1 1.3 論文架構. . . . . 2 第二章 相關研究與背景知識 2.1 延遲錯誤. . . . . 3 2.2 掃描鏈. . . . . 4 2.3 內建式自我測試. 6 2.4 實速測試方法. . . . . 6 2.4.1 不對稱負載方法 . . . . 7 2.4.2 寬邊方法 . . . . 8 2.5 鎖相迴路與延遲鎖定迴路. . . . . 9 2.6 同步鏡像延遲. . . . . 9 2.7 相位校正緩衝器. . . . . 11 第三章 電路架構設計 3.1 內嵌式掃描延遲量測與測試電路架構 . . . . 13 3.2 時間延遲量測與測試電路設計 . . . . 15 3.2.1 相位差偵測與振盪器. . . . . 16 3.2.2 相位偵測電路. . . . . 17 3.2.3 量測控制致能產生器. . . . . 18 3.2.4 計數器. . . . . 18 3.2.5 資料壓縮電路. . . . . 19 3.2.6 D 型正反器. . . . . 19 第四章 實驗模擬結果與晶片設計 4.1 時間延遲量測與測試電路模擬結果. . . . . 21 4.2 晶片實作 . . . . 33 4.2.1 設計流程. . . . . 33 4.2.2 預計規格. . . . . 34 4.2.3 測試考量. . . . . 35 4.2.4 佈局平面圖與打線圖. . . . . 36 4.3 模擬測試 . . . . 39 4.4 電路測試 . . . . 39 第五章 標準元件庫概論與元件特徵值萃取方法及模型建立 5.1 標準元件庫 . . . . 42 5.2 元件實體佈局 . . . . 42 5.3 邏輯資訊 . . . . 44 5.4 時序資訊 . . . . 44 5.5 功率資訊 . . . . 49 5.6 標準元件庫建立流程簡介 . . . . 51 5.7 特徵值萃取及模型建立流程簡介 . . . . 52 5.8 特徵值種類及其萃取原理 . . . . 53 5.8.1 Pin to Pin Delay . . . . 53 5.8.2 Power Consumption . . . . 56 5.8.3 Input Capacitance . . . . 61 5.8.4 Time Constraints of Sequential Circuit . 62 5.9 標準元件庫模型的建立 . . . . 63 5.9.1 Verilog model. . . . . 63 5.9.2 Synopsys model . . . . 64 第六章 動態邏輯電路的標準元件庫建構 6.1 動態邏輯電路 . . . . 66 6.2 標準動態元件庫建構 . . . . 67 6.3 MOS 的尺寸調整設計 . . . . 71 6.4 特徵值萃取與模型建立 . . . . 77 第七章 結論與討論. 79 參考文獻. 81

REFERENCES

[1.] Kihyuk Sung; Lee-Sup Kim; “ A high-resolution synchronous mirror delay using successive approximation register ”, Solid-State Circuits, IEEE Journal of Volume 39, Issue 11,Nov. 2004 Page(s):1997 - 2004 [2.] Datta, R.; Sebastine, A.; Abraham, J.A.; “ Delay fault testing and silicon debug using scan chains ”, Test Symposium, 2004. ETS 2004. Proceedings. Ninth IEEE European 23-26 May 2004Page(s):46 – 51 [3.] Srinivas Patil; “ AC-Scan: Microprocessors are ready. But Where is the Infrastructure? ”, Proceedings of the International Test Conference 2001 (ITC01) [4.] Seongmoon Wang; Xiao Liu; Chakradhar, S.T.; “ Hybrid delay scan: a low hardware overhead scan-based delay test technique for high fault coverage and compact test sets Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings Volume 2, 16-20 Feb. 2004 Page(s):1296 - 1301 Vol.2 [5.] Kuo-Hsing Cheng; Yung-Hsiang Lin; “ A dual-pulse-clock double edge triggered flip-flop for low voltage and high speed application ” Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on Volume 5, 25-28 May 2003 Page(s):V-425 - V-428 vol.5 [6.] Bhaskar Chatterjee; Manoj Sachdev; Keshavarzi, A.; “ DFT for delay fault testing of high-performance digital circuits ” Design & Test of Computers, IEEE Volume 21, Issue 3, May-June 2004 Page(s):248 - 258 [7.] Young, I.A.; Greason, J.K.; Wong, K.L.; “ A PLL clock generator with 5 to 10 MHz of lock range for microprocessors ” Solid-State Circuits, IEEE Journal of Volume 27, Issue 11, Nov. 1992 Page(s):1599 - 1607 [8.] Dunning, J.; Garcia, G.; Lundberg, J.; Nuckolls, E.; “ An all-digital phase-locked loop with 50-cycle lock time suitable for high-performance microprocessors ” Solid-State Circuits, IEEE Journal of Volume 30, Issue 4, April 1995 Page(s):412 – 422 [9.] Shin-Moe Wang ; Chang-Wen Wu ；“ Test Integration of Core-Based System-on Chip Supporting Delay Test ” 國立清華 大學電機工程研究所碩士論文 [10.]Design for testability with DFT compiler and TetraMax ” training manual 國家晶片系統設計中心,2004.0 [11.]陳麒旭,國家晶片系統設計中心設計服務組, ” 標準元件庫 (Standard Cell Library)概說 ”, IC design 月刊2002.10 號 P28~P36.
[12.]郭建興,工研院系統晶片技術中心,“ 標準元件庫特徵值萃取與模型建立 ”, IC design 月刊 2003.01 號 P44~P56.
[13.]謝明得,雲林科技大學 ” 數位系統電路後段設計流程整合實務--Standard Cell Library Creation ” ,教育部顧問室[超大型積體 電路與系統設計]教育改進計劃P&L 聯盟教材.
[14.]鄭經華,王進賢,張世杰,李信德,楊政輝,中正大學 “ Domino logic compiler ” ,87 學年度大專校院 Silicon Intellectual Property 創作競賽.
[15.]簡丞星,U100/CCL/ITRI, “ 標準元件庫特徵化程式使用者手冊 User ’ s Guide of Characterization Utilities Revision 1.0 ” ,April 19 1996.
[16.] 莊英廷同學/ 交通大學電控所 蘇朝琴教授指導, “ 625Mhz 低功率小面積全數位相位校正緩衝器 ”,國家晶片系統設計中心 2005 晶片製作成果發表會 [17.]葉有偉同學 /中正大學電機所 王進賢教授指導, “ 新型低功率全數位式脈波寬度鎖定迴路 ”,國家晶片系統設計中心2005 晶 片製作成果發表會 [18.]陳俊良, “ 一個基於路徑延遲慣量之新延遲障礙測試方法 ” 國立交通大學電子工程研究所碩士論文 [19.]林森田, “ 單時脈電路的掃瞄設計與測試 ”,國立中正大學資訊工程研究所碩士論文 [20.]牛風舉, 明導(上海)電子科技有限公司, “ 可測試性設計與EDA 技術 ” 《電子工程專輯》網站: http://www.eettaiwan.com/article/article_content.php3?article_id=8800326568 [21.]Ron Press, Mentor Graphics, Wilsonville; “ Smart test for nanometer designs ” Test & Measurement World , 10/1/2004 ; http://www.reed-electronics.com/tmworld/