

ESD/TLP Measurement Instruments and ESD Immunity Analysis in the Electronic Device

王光一、陳勝利 許崇宜

E-mail: 9419813@mail.dyu.edu.tw

ABSTRACT

Reliability engineer of integrated circuit occupies a most important position when the accuracy of process got better and better . The improvement of the technical procedure will enhance the reliability of integrated circuit in design. There is another element to effect the reliability engineer when we enhances the yield. Though one of the factors is the ESD of destruction.it can be avoidable. There are many productions of the protection circuit of ESD in academic.but ESD protect the circuit and some elements which protect the circuit are often effected by the efficiency of ESD stress cause the circuit protection is useless. The reliable of the circuit protection element is queried. The thesis will use some ESD protection Devices to do ESP testing. Analyze anti ESD ability. Pick up element to avoid latch up effect . To analyze the reliable ability and ESD energy. we can use the TLP and ESD instruments which is similar to ESD stress to test the anti-static electricity ability. Prote element can maintain the voltage effectively. When the element of voltage value enter the collapse point effectively and maintain appropriate capacity of releasing the ESD. Furthermore, it also prevent the coming of second collapse point effectively. Therefore how to find and the first and second appropriate collapse point is very impertant. Analyzing the static electricity workable or not in a circuit.

Keywords : Reliability.collapse point

Table of Contents

封面內頁 簽名頁 授權書	iii	中文摘要	iii
. iv 英文摘要	iv	v 誌謝	v
. vi 目錄	vi	vii 圖目錄	vii
. x 表目錄	x	xiii 第	xiii
第一章 緒論 1.1 靜電放電問題	1	1.2 保護靜電破壞電路元件	2
1.3 測試儀器 :傳輸線觸波產生系統	3	1.4 論文架構	3
第二章 靜電放電 2.1 靜電放電的成因	4	2.2 靜電放電破壞機制	5
放電模型	5	2.2.1 人體	5
2.2.2 機器放電模型	9	2.2.3 元件放電模型	9
. 10	10	2.2.4 電場感應模型	11
2.3 靜電放電測試組合與程序	11	2.3.1 靜電放電測試組合	11
2.3.2 I/O PIN的靜電放電測試	11	2.3.3 PIN	11
TO PIN 的靜電放電測試	12	2.3.4 VDD-to-VSS 的靜電放電測試	13
2.3.5 Analog pin的靜電放電測	14	2.3.6 靜電放電測試故障臨界	15
試	14	2.4 靜電放電測試判定標準	16
2.5 靜電放電測試結果判讀	17	第三章 靜電放電保護電路基本元件 3.1 靜電放電保護電路概念	19
.	19	3.2 電阻	20
.	21	3.3 二極體	21
.	21	3.4 雙載子接面電晶體	23
.	26	3.5 金屬半場效電晶體	23
.	26	3.6 矽控整流器	29
.	29	3.7 瞬間突壓抑制器	33
第四章 ESD/TLP量測儀器 4.1 研究量測儀器: ATLP	35	4.1.1功能	35
.	35	4.1.2 保護電路的元件	35
.	36	4.1.3 來源	36
.	36	4.1.4 原理與	36
工作	36	4.1.5 觀察與判斷	39
.	40	4.2 分析討論	39
.	40	第五章 測試結果與討論 5.1 測試方法	43
.	44	5.2 用TLP測試結果	43
.	44	5.3 IC定點橫切面	51
.	61	第六章 結論	51
.	61	參考文獻	62
.	61	62

REFERENCES

- [1] "American nation standard guide for electrostatic discharge test methodologies and criteria for electronic equipment" accredited standards committee on electromagnetic compatibility , c63 , USA. [2] 柯明道,陳東陽 "次微米互補式金氧半積體電路之靜電防護" CCL TECHNICAL JOURNAL 9.5,PP.85-96 1997. [3] MIL-STD-883C method 3015.7, "Military Standard Test Methods and Proc.for Microelectronics" ,Dept.of defense,Washington,D.C.,U.S.A.,1989. [4] JEDC STANDARD JESD22-A114-B " Electroststic Discharge (ESD)

Sensitivity Testing Human Body Model(HBM).” JEDEC SOLID STATE TECHNOLOGY ASSOCIATION,june 2000. [5] JEDC STANDARD JESD22-A114-B “ Electrostatic Discharge (ESD) Sensitivity Testing Machine Model(MM).” JEDEC SOLID STATE TECHNOLOGY ASSOCIATION,june 2000. [6] 李文明, “功率MOS元件ESD破壞可靠性分析之研究” 大葉大學,2000 [7] 朱季齡, “功率MOS元件ESD破壞可靠性分析之研究” 大葉大學,2000 [8] 柯明道, “次微米互補式金氧半積體電路之靜電防護-全晶片防護設計篇”,電腦與通訊,第62期,pp.67~83,1997 [9] 李文明, “功率電晶體IC之ESD破壞分析及保護電路設計”,電力電子技術月刊,pp.220-226,2000 [10] 李文明, “積體電路高容值I/O埠抗ESD靜電破壞能力之量測” 電子月刊,vol.6,no.4,pp.220-226,2000 [11] 黃致遠, “靜電放電保護電路設計與門鎖效應防制之研究” 大葉大學,2002