# The Study of the Poly-Silicon Gate Stress Induced Threshold Voltage Shift In 90 Nano Device

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**ABSTRACT**

CMOS (Complementary Metal Oxide Semiconductor) devices applied to System on Chip (SOC) is becoming a trend in the future, and the most key technologies are how to grow up the different oxide thickness and how to accept the various bias voltages in IC operation. In order to enable the general logic circuits to reach a better operation state, the reliability issues and the circuit structures need to be integrated and evaluated . A deep sub-micron MOSFET is the most advanced product of coming nano device generation. Meanwhile, the ultra-thin gate oxide layer of this nano scale device brings lots of issues and bottlenecks in device processing, design, performance modeling, characterization, parameter extraction and so forth. This thesis of discussions to describe and characterize the nano device ’ s characteristics, inclusive of high gate oxide leakage current, tunneling leakage current, punch-through current, I-V & C-V behaviors, reliability, stress condition, temperature dependence effect, frequency dependence effect and so on. We know, in/after 90nm manufacturing generation, there will be more and more technology skills and key-issues waiting for us to improve even completely solution. Hope our research results could provide some contribution to the final nano-issued-solution especially on ultra thin gate oxide leakage issue.

Keywords : CMOS (Complementary Metal Oxide Semiconductor)、System on Chip (SOC)、oxide thickness

**Table of Contents**



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