Low Power Domino Circuit Design

邱威豪、林浩仁

E-mail: 9418562@mail.dyu.edu.tw

ABSTRACT

With the advanced processing, the difference region between supply voltage and threshold voltage is scaled gradually. The scaled noise margin causes the leakage current to be one of the critical issues in the very deep submicron designs, and will seriously cause unnecessary power consumption. Domino keeper is always using to keep the noise margin in high fan-in domino gate. However, both the increasing power consumption and slower performance are significant problems due to the causing DC contention. In this paper, we present a new high-speed domino technique, called Conditional Isolator Domino (CI-Domino) , for wide fan-in domino logic. The CI-Domino logic not only improves the noise margin without sacrifices performance, moreover, subthreshold current can be significantly reduced in CI-Domino operations. By the simulation results on 0.18 μm processing, CI-Domino significantly achieves the 48.14% noise margin improvement respective to conventional domino in the comparison of 32 fan-in OR gate, and further, CI-Domino reduces active power by 49.14%, standby power by 35.99%, and delay time by 60.27%.

Keywords : Noise Margin, Leakage Current, Domino Logic Circuit, DC Contention, Subthreshold Current, Dynamic Power, Static Power, Delay time.

Table of Contents

REFERENCES

[1] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, “ Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits, ” in Proc. of IEEE, pp. 305-327, Vol. 91, no. 2, Feb. 2003.

[2] A. Dancy and A. Chandrakasan, “ Techniques for aggressive supply voltage scaling and efficient regulation, ” in Proc. of 1997 Custom Integrated Circuit Conference, pp. 579-586, May. 1997.

[3] M. Anders, R. Krishnamurthy, R. Spotten, and K. Soumyanath, “ Robustness of sub-70 nm dynamic circuits: analytical techniques and scaling trends, ” in Proc. of 2001 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 23-24, June. 2001.

[4] J. Kao, S. Narendra, A. Chandrakasan, “ Subthreshold leakage modeling and reduction techniques, ” in Proc. of the ICCAD 2002, pp. 141 -148, Nov. 2002.

[5] Y. F. Tsai, N. Vijaykrishnan, Y. Xie, and M. J. Irwin, “ Influence of leakage reduction techniques on delay/leakage uncertainty, ” in Proc. of 18th International Conference on VLSI Design, pp. 374-379, Jan. 2005.

[6] B. J. Sheu, et al., “ BSIM: Berkeley Short-Channel IGFET model for MOS Transistors, ” IEEE J. Solid-State Circuits, Vol. -52-22, pp. 558-566, Aug, 1987.

[7] R. H. Krambeck, C. M. Lee, H. F. S. Law, “ High-Speed Compact Circuits with CMOS, ” IEEE J. Solid-State Circuits, SC-17(3), pp.614-619, June, 1982.

[8] Z. P. Chen, M. Johnson, L. Wei, and W. Roy, “ Estimation of standby leakage power in CMOS circuit considering accurate modeling of transistor stacks, ” in Proc. of International Symposium 1998 on Low Power Electronics and Design, pp. 239-244, Aug. 1998.

[9] W. Jiang, V. Tiwari, E. de la Igtesia, and A. Sinha, “ Topological analysis for leakage prediction of digital circuits, ” in Proc. of ASP-DAC 2002, pp. 39-44, Jan. 2002.

[10] Y. Liu and Z. Gao, “ Timing analysis of transistor stack for leakage power saving, ” in Proc. of 9th International Conference on Electronics, Circuits, and Systems, Vol. 1, pp. 41-44, Sept. 2002.
[11] S. Yang, W. Wolf, N. Vijaykrishnan, Y. Xie, and W. P. Wang, “ Accurate stacking effect macro-modeling of leakage power in sub-100 nm circuits, ” in Proc. of 18th International Conference on VLSI Design, pp. 165-170, Jan. 2005.
[12] M. Anis, S. Areibi, M. Mahmoud, and M. Elmasry, “ Dynamic and leakage power reduction in MTCMOS circuits using an automated efficient gate clustering technique, ” In Proc. DAC, pp. 480-485, June. 2002.
[13] C. Long and L. He, “ Distributed sleep transistor network for power reduction, ” IEEE Transactions on Very Large Scale Integration System, Vol. 12, No. 9, pp. 937-946, Sept. 2004.
[14] B. Chatterjee, M. Sachdev, and R. Krishnamurthy, “ Leakage control techniques for designing robust, low power wide-OR domino logic for sub-130nm CMOS technologies, ” in Proc. of 5th International Symposium on Quality Electronic Design, pp. 415-420, March. 2004.
[15] V. Kursun and E. G. Friedman, “ Node voltage dependents subthreshold leakage current characteristics of dynamic circuits, ” in Proc. of 5th International Symposium on Quality Electronic Design, pp. 104-109, March. 2004.
[16] K. Christine, C. Bhaskar, and S. Manoj, “ Modeling and Designing Energy-Delay Optimized Wide Domino Circuits, ” in Proc. of ISCAS ’ 04 on VLSI Systems and Applications: Digital VLSI Circuits, Vol. 2, pp. 921-924, May. 2004.
[17] A. Alvandpour, P. Larsson-Edefors, and C. Svensson, “ A leakage-tolerant multi-phase keeper for wide domino circuits, ” in Proc. of 1999 International Conference on Electronics, Circuits and Systems, Vol. 1, pp. 209-212, Sept. 1999.
[18] A. Alvandpour, R. Krishnamurthy, K. Soumyanath, S. Borkar, “ A Conditional Keeper Technique for Sub-0.13mm Wide Dynamic Gates, ” in Proc. of 2001 International Symposium -54-on VLSI Circuits, pp. 29-30, June. 2001.
[19] A. Alvandpour, R. Krishnamurthy, K. Soumyanath, S. Borkar, “ A Sub-130nm Conditional Keeper Technique, ” IEEE Journal of Solid-State Circuits, Vol. 37, No. 5, pp. 633-638, May. 2002.
[20] M. W. Allam, M. H. Anis, and M. I. Elmasry, “ High-speed dynamic logic styles for scaled-down CMOS and MTCMOS technologies, ” in Proc. of 2000 International Symposium on Low Power Electronics and Design, pp. 155-160, 2000.
[21] M. H. Anis, M. W. Allam, and M.I. Elmasry, “ Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies, ” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 2, pp. 71-78, Apr. 2002.
[22] S. O. Jung, S. M. Yoo, K. W. Kim, and S. M. Kang, “ Skew-tolerant high-speed (STHS) domino logic, ” in Proc. of International Symposium 2001 on Circuits and Systems, Vol. 4, pp. 154-157, May. 2001.
[23] S. O. Jung, K. W. Kim, and S. M. Kang, “ Optimal timing for skew-tolerant high-speed domino logic, ” in Proc. of IEEE Computer Society on Annual Symposium, pp. 34-39, April. 2002.
[24] Kwang-II Oh and L. S. Kim, “ A clock delayed sleep mode domino logic for wide dynamic OR gate, ” in Proc. of ISLPED ’ 03 on Low Power Electronics and Design, pp. 176-179, Aug. 2003.
[25] G. Yang, Z. D. Wang, and S. M. Kang, “ Low power and high performance circuit techniques for high fan-in dynamic gates, ” in Proc. of 5th International Symposium on Quality Electronic Design, pp. 421-424, 2004.
[26] S. J. Shieh, J. S. Wang, and Y. H. Yeh, “ A contention-alleviated static keeper for high-performance domino logic circuits, ” in Proc. of ICECS 2001, Vol.2, pp.707-710, Sept. 2001.
[27] Y. J. Xu, Z. Y. Luo, Z. G. Chen, and X. W. Li, “ Average leakage current macro modeling for dual-threshold voltage circuits, ” in Proc. of 12th Asian Test Symposium, pp. 196-201, Nov. 2003.
[28] J. S. Wang, C. R. Chang, and C. W. Yeh, "Analysis and Design of High-Speed and Low-Power CMOS PLAs, " IEEE Journal of Solid-State circuits, Vol. 36, No. 8, pp. 1250-1262, Aug. 2001.
[29] J. M. Chang and M. Pedram, “ Energy Minimization Using Multiple Supply Voltages, ” IEEE Transactions on Very Large Scale Integration Systems, Vol. 5, No. 4, pp. 436-443, Dec. 1997.
[30] V. Sandararajan and K. K. Parhi, “ Synthesis of low power CMOS VLSI circuits using dual supply voltages, ” in Proc. of DAC, pp. 72-75, June. 1999.
[31] J. Cai, Y. Taur, S. F. Huang, D. J. Frank, S. Kosonocky, and R. H. Dennard, “ Supply voltage strategies for minimizing the power of CMOS processors, ” VLSI Technology, pp. 102-103, June. 2002.
[32] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, J. Yamada, “ 1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS, ” IEEE J. Solid-State Circuits, Vol. 30 No. 8, pp. 847 -854, Aug. 1995.
[33] H. S. Won, K. S. Kim, K. O. Jeong, K. T. Park, K. M. Choi, J. T. Kong, “ An MTCMOS design methodology and its application to mobile computing, ” in Proc. of ISLPED ’ 03, pp. 110-115, Aug. 2003.
[34] K. Usami, N. Kawabe, M. Koizumi, K. Seta, and T. Durusawa, “ Automated Selective Multi-Threshold Design for Ultra-Low Standby Application, ” in Proc. of ISLPED ’ 02, pp. 202-206, Aug. 2002.