低功率消耗之骨牌式電路設計

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摘 要

隨著製程技術的進步，深次微米與奈米電路的工作電壓值與臨界電壓值的差距區間(即雜訊邊界)逐漸變小，使得電路的漏電流問題變得更為嚴重，造成更多不必要的功率消耗，並且影響電路的雜訊免疫能力。 對於多輸入的骨牌式(Domino)邏輯閘，更大的充電電晶體通常被用來保持電路的雜訊邊界，然而所造成的 充放電競局(DC Contention)現象將嚴重影響電路速度與功率損失；在避免造成充放電競局現象的前提下，如何降低上升的功率消耗以及較慢的運算速度，是相當關鍵的議題。在本篇論文中，我們提出了 Conditional Isolator Domino (CI-Domino)電路設計技術，CI-Domino適用於較多輸入(High Fan-in) 的高速骨牌式電路設計。CI-Domino除了可以在不犧牲電路速度的前提下，明顯改善電路的雜訊邊界之外，也可以同時將電路的次臨界電流減小。以32輸入的OR閘為例，根據0.18μm製程的電路模擬結果， CI-Domino相較於傳統統骨牌式電路結構，在雜訊邊界的改善達到了30.76%；並且，CI-Domino能夠減少 43.7%的動態耗能、33.96%的靜態耗能、以及60.38%的延遲時間。

關鍵詞 : 雜訊邊界，漏電流，骨牌式邏輯閘，充放電競局，次臨界電流，動態耗能，靜態耗能，延遲時間

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