A High-Performance/Low-Power Mixed Static/Dynamic Circuit Synthesizer

葉重廷、鄭經華 ; 林浩仁

E-mail: 9418561@mail.dyu.edu.tw

ABSTRACT

Because domino logic design offers smaller area and higher speed than complementary CMOS design, it has been very popularly used to design high-performance processors. There are several research works on high-performance mixed static/dynamic circuit; but most of the works focus on the theory discussion without practical results are presented. In this thesis we try to establish the cell based design flow of the mixed/merged static/dynamic circuit synthesis, which has skew tolerant, low-power and high-performance characteristics. And, the real chip implementation and silicon proven will be validated finally. In this work, there is three major targets are got: Target-one, we propose a static-dynamic-static(SDS)high-performance/low-power mixed/merged static/dynamic circuit design techniques. Target-two: the supported synthesizable design flow has been established for Target-one; we focus on the skew-tolerant issue of this target by using current CAD tools. Target-three, two noise-alleviation (charge sharing, crosstalk) domino cell libraries are generated to support the cell-based synthesis CAD design tools. Key word：mixed/merged，static circuit ，dynamic circuit，cell base

Keywords : mixed/merged ; static circuit ; dynamic curcuit ; cell base

Table of Contents

REFERENCES

[1] M. R.Prasad, D.Kirkpatrick, and R. K.Brayton,“ Domino logic synthesis and technology mapping,” presented at the Workshop Notes. Int. Workshop Logic Synthesis, 1997.

[2] T.Thorp, G.Yee, and C.Sechen,“ Domino logic synthesis using complex static gates,” in Proc. IEEE/ACM Int. Conf. Computer-Aided Design, 1998, pp. 242-247.

[3] .Puri, A.Bjorksten, and T. E. Rosser,“ Logic optimization by output phase assignment in dynamic logic synthesis,” in Proc. IEEE/ACM Int. Conf. Computer-Aided Design, 1996, pp. 2-8.

[4] D.Harris and M. A.Horowitz,“ Skew-tolerant domino circuits,” IEEE J. Solid-State Circuits, vol. 32, pp. 1702-1711, Nov. 1997.

[5] R.Puri,“ Design issues in mixed static-domino circuit implementations,” in Proc. IEEE Int. Conf. Computer Design, 1998, pp. 270-275.

[6] T.Williams,“ Dynamic logic: Clocked and asynchronous,” in Tutorial notes Int. Solid-State Circuits Conf., 1996.

[7] Clock-delayed domino for dynamic circuit design Gin Yee; Sechen, C.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 8, Issue 4, Aug. 2000 Page(s):425 - 430