Implementation of DC/DC Converter Driver IC

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ABSTRACT

In order to reduce the power consumption the SOC(system on chip) design usually needs to use the different voltage levels. Moreover, the variable frequency technology is employed to change the frequency for the different function. Thus the power consumption can be reduce by using slow clock in low frequency circuits. Such variable voltage/variable frequency power management strategy is more important in the modern power management chip design. Therefore, in this paper, we employed a new variable voltage/variable frequency PWM(pulse-width modulation) circuit design. The variable voltage/variable frequency sawtooth generator (sawtooth oscillatior) is used to produce a stable sawtooth waveform in this paper. Moreover, some protection function is designed to fit the industrial requirements. This circuit is implemented by the 0.35 μ m processing of TSMC (Taiwan Semiconductor Manufacture Company). It can operate from 500KHz to 3MHz, supply voltage is 3.3V, total area is 0.436*0.436m2, and the power consumption is 4mW. From the simulation results, this excellent performance of the variable voltage/variable frequency PWM chip is verified.

Keywords : 系統晶片 ; 電源管理晶片 ; 脈波寬度調變器

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