The Circuit Path Delay Identification Framework

沈威志、鄭經華 ; 林浩仁

E-mail: 9418546@mail.dyu.edu.tw

ABSTRACT

IR-drop is a well-known signal integrity issue in very deep submicron technology. The voltage drop does not only induce circuit delay but also reduce the circuit noise margin from lower supply voltage and bring reliability issue from electromigration. In this thesis, there are two maximum transition current estimation methods are discussed, Method-1 is pattern independent, which is worst-case predication. The Method-2 is pattern independent that more realistic than Method-1. The real circuit transition current could get by applying the verification input patterns provided by designer. Due to the peak current overestimated by using Method-1, and the accurate peak current is dynamic behavior（dependent on pattern）, so use real test bench could activate real gate transitions peak current. This measurement might lower and accurate than Method-1, could help reasonable power rail design. Traditional static timing analysis（STA） does not consider the different gate delay when occur varying supply voltage. We find a simple circuit ’s delay increase up to 14.7% when voltage drop to 0.78Vdd. In this thesis, we propose a voltage aware delay calculation framework, which combine the peak current calculation and the path delay induced computation, the methodology will recompute the path delay, which take the voltage drop factors into consideration. The accurate（current, voltage, delay） library are characterized and calibrated by using SPICE. This proposed framework could analyze how serious of voltage drop from the circuit, and joint with the gate-sizing/input-reordering peak-current reduction techniques finally.

Keywords : IR-drop ; Peak Current ; Voltage Drop ; delay

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