Peak Current Reduction by Using Useful Skew/Slack

賴永浩、鄭經華 ; 林浩仁

E-mail: 9418545@mail.dyu.edu.tw

ABSTRACT

IR-drop is a well-known signal integrity issue in very deep submicron technology. The voltage drop does not only induce circuit delay but also reduce the circuit noise margin from lower supply voltage and bring reliability issue from electromigration. In this thesis, there are two maximum transition current estimation methods are proposed, Method-1 is pattern independent, which is worst-case predication. The Method-2 is pattern dependent that more realistic than Method-1. The real circuit transition current could get by applying the verification input patterns provided by designer. Due to the peak current overestimated by using Method-1, and the accurate peak current is dynamic behavior (dependent on pattern), so use real test bench could activate real gate transitions peak current. This measurement might lower and accurate than Method-1, could help reasonable power rail design. The peak current could be reduced from lower the input/output transition slew time [14]. The input signal slew rate not only affects the gate delay but also contribute the peak current to a gate. So, the lower input/output slew time could reduce the peak current, but need to make sure do not affect the circuit performance first. We discuss the gate-sizing/input-reordering might be the practical techniques in this thesis. Each gate output signal slew rate represented by gate driving capability, so the gate-sizing technique will choose the same function gate has less driving capability from cell library during logic synthesis phase. The input-reordering technique will lower the input/output slew time to minimum the peak current by applying the control/non-control signal relationships. The experimental results show the gate-sizing/input-reordering techniques are feasible solutions for reducing peak current without circuit delay increased.

Keywords : Gate Resizing ; Input Reordering ; IR-Drop

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